SELECTIVE DRY ETCH FOR DEFINING OHMIC CONTACTS FOR HIGH PERFORMANCE ZnO TFTs

THESIS

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Abstract

Recently, gigahertz RF performance has been demonstrated in zinc oxide (ZnO) TFT. However, the need arises for sub-micron channel length (L_c) dimensions to extend these results into X-band frequency range of operation. This thesis is a pioneering effort identifying device access materials to be selectively etched to ZnO via plasma-assisted etch (PAE) to avoid processing limitations from traditional optical lithography channel definition methods. A subtractive etch process using CF_4/O_2 gas mixture was completed with various Ohmic contact materials to ZnO providing foundational research upon which nano-scale, high-frequency ZnO thin-film transistors (TFTs) could be fabricated. Molybdenum, tantalum, titanium tungsten 10-90, and tungsten metallic contact schemes to ZnO are investigated for their etch selectivities to ZnO and etch profiles. Tungsten displayed promising device scalability results with excellent aspect ratio and 200nm L_c. A new semiconductor-semiconductor contact interface to ZnO using nc-Si is initially reported with 15mA/mm current density and 18mS/mm transconductance. Nc-Si also displays promising scaling results through the subtractive etch process defined with e-beam lithography. Results included 157nm channel length, high aspect ratio, and high extrapolated current density of nearly 1A/mm at 100nm L_c and gate and drain voltages of 10V.

To my sister, my family, and many friends
for their love, prayers, and support

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Matthew L. Herold

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List of Symbols

Symbol	Definition
Å	ångström (10^{-10} meter)
°C	degrees, Celsius (0°C = 273.2 Kelvin)
c_g	capacitance, gate
X_{SC}	electron affinity, semiconductor
eV	electron-Volts
f_t	frequency, unity current gain
g_m	transconductance, small-signal
g'_m	transconductance, effective
L_c	length, channel
μm	micron, micrometer (10^{-6} meter)
n	carrier concentration (cm^{-3}), n-type
nm	nanometer (10^{-9} meter)
Φ_M	work function, metal
Φ_{SB}	work function, Schottky barrier
Φ_{SC}	work function, semiconductor
r_{ss}	resistance, small-signal (access or source)
q	charge (eV)
ρ	resistivity (Ω-cm)

Symbol	Definition
ρ_c	resistivity, contact (Ω-cm^2)
ρ_s	resistivity, sheet (Ω-cm)
V	Volt
W	Watt
W_c	width, channel

List of Acronyms

Acronym	Definition
AFRL	Air Force Research Laboratory
AMLCD	active-matrix liquid-crystal display
BJT	bipolar junction transistor
CD	critical dimension
CVD	chemical vapor deposition
d.u.	dimensionless unit
DC	direct current
DI	deionized water
DRIE	deep reactive-ion etching
DUV	deep ultra-violet
e-beam	electron beam
ER	etch rate
FIB	focused ion beam
IC	integrated circuit
ICP	inductively-coupled plasma
LED	light-emitting diode
MBE	molecular beam epitaxy
MMIC	monolithic microwave integrated circuit
MOCVD	metal-organic CVD
MOSFET	metal-oxide-semiconductor field-effect transistor
nc-Si	nanocrystalline silicon
NMOS	n-channel MOSFET
OE	over-etch

Acronym	Definition
PAE	plasma-assisted etch
PBS	poly-butene-1 sulfone
PECVD	plasma-enhanced chemical vapor deposition
PLD	pulsed-laser deposition
PMGI	polydimethylglutarimide
PMMA	poly-methyl methacrylate
PR	photoresist
RF	radio frequency
RIE	reactive-ion etching
RT	room temperature
RTSE	real time spectroscopic ellipsometry
SEM	scanning electron microscope
TFT	thin-film transistor
TLM	transmission line model
UV	ultra-violet

SELECTIVE DRY ETCH FOR DEFINING OHMIC CONTACTS

FOR HIGH PERFORMANCE ZnO TFTs

I. Introduction

1.1 Background

THROUGHOUT the previous century since their invention, solid-state transistors have been subjected to multiple iterations of design modification and material selection. Originally patented in 1934 by Lilienfeld [23], the first transistor design took the form of thin-film and was comprised of a Cu_2S semiconducting layer, with Al_2O_3 insulator material and an aluminum gate. In the following year, Heil patented a transistor design [8] based on tellurium. Although these devices were only theorized and never constructed, they were later improved in design and materials by Shockley in 1940 [23] at Bell Laboratories with a germanium semiconducting active layer. Citing insufficient knowledge of semiconductor physics and thus poor device performance, Shockley began characterizing the surface states of elemental semiconductors such as germanium and silicon and thus further quantifying their quantum mechanics. This research, while noble and pioneering, resulted in the abandonment of thin-film device characterization and fabrication [65] and led to the creation of the bipolar junction transistor (BJT) by 1950.

The thin-film transistor (TFT) would not return until the late 1960s, when Brody [8] discovered its usefulness in his invention, the large-format, active-matrix liquid-crystal

displays (AMLCDs). During this time period, the silicon metal-oxide-semiconductor field-effect transistor (MOSFET) also received considerable attention and became the desirable device for solid-state research [8, 23] due to its promising performance and low-cost fabrication. As the popularity of characterizing the MOSFET continued, Brody and his research group garnered much criticism for wasting research dollars on the TFT. Despite this criticism, they persisted in their research and produced the first TFT-addressed, AMLCD in 1973, with a CdSe semiconducting layer. Shown in Figure 1.1, the first TFT-addressed AMLCD achieved 20 line-per-inch resolution on a 6”x6” display panel. When suitable deposition methods for TFT fabrication of amorphous-Si were discovered in 1979, the AMLCD was revolutionized as cost-effective and high-performance devices [23] were realized compared to their bulk- and poly-Si counterparts. As a result, the TFT is widely used in the multi-billion-dollar television industry today [22].

However, little research has been focused on discovering new applications for TFTs outside of the flat-panel industry. TFTs are well known for their ability to be fabricated across large areas [22], whereas most transistors utilized in today’s integrated circuits (ICs) must be smaller. Furthermore, these large-format display applications operate with low-current and low-frequency when compared to existing ICs. While some transistor types and their particular material composition exhibit the ability to operate high-current and high-frequency switching, researchers are driven to discover new permutations of designs and materials to meet the perpetual need for devices which are cheaper to manufacture, easier to fabricate, and have better performance characteristics.

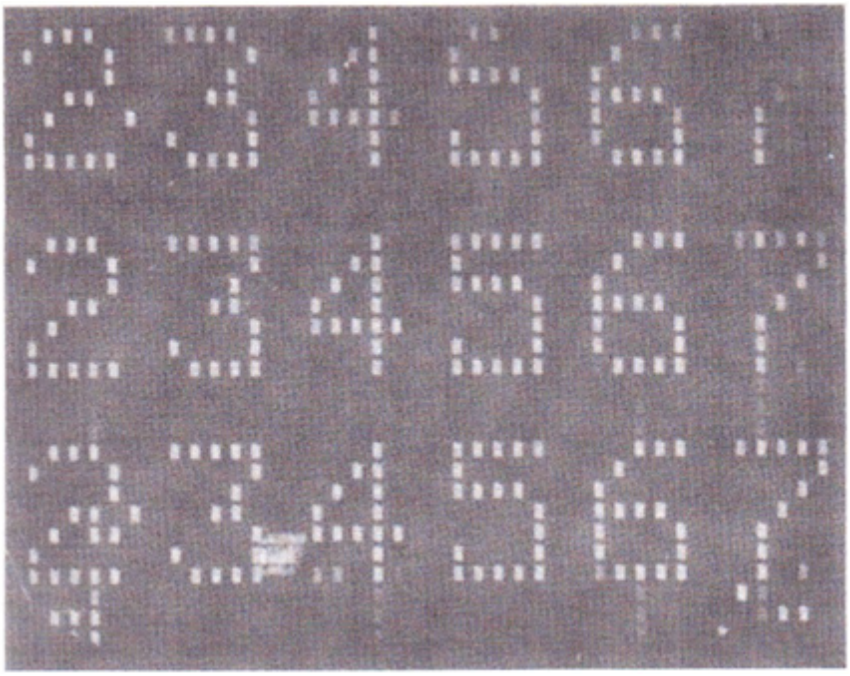

Figure 1.1: The first TFT-addressed AMLCD [8]

1.2 Problem Statement

A material that has received considerable attention in the past 15 years is ZnO, for its application as the active conducting layer of transistors. ZnO is not a new semiconducting material; it has been studied for many decades with varying interest as viable microelectronics fabrication technologies have been either unattainable or newly developed [49]. Since 2000 B.C., the material ZnO has been used in facial powder and medical ointments [15], and within the last century sunscreens, paint pigmentation, and rubber, the latter of which accounts for 50-60% of global production of ZnO today [41]. As a result, its material properties have been well-defined over this time period.

Single-crystal bulk ZnO substrates have been available for many decades, but current native epitaxial growth progress has slowed due in part to their high cost [27].

The present surge in interest of ZnO arises from discovery of nanocrystalline- and amorphous-ZnO thin-films exhibiting similar electrical performance to their single-crystal growth counterparts [2, 11, 21, 49]. Additionally, microwave performance in nanocrystalline ZnO devices has been recently demonstrated and it is further hypothesized X-band operation would be attainable through applying gate-length scaling [2]. Microwave performance is notable because most TFT applications have little demand for high-frequency operation [1, 23]. Such high frequency operation is dependent on several device parameters, of which non-rectifying (Ohmic) device access materials become more important as critical dimensions (CDs) shrink [7]. Ohmic contact definition on ZnO TFTs can be achieved by lift-off, wet chemical etching or dry etching various materials. Lift-off processes, known as having a low degree of pattern control, are damaging to the ZnO surface. Wet etching processes are further complicated in fabrication of ZnO TFTs due to ZnO's inherent sensitivity to most common wet-etchants. To obtain small geometries required for high-frequency device performance, a good selective dry etch method must therefore be used in which damage to the ZnO nanocrystalline structure is minimized. To date, selective dry-etch processes for Ohmic contacts to ZnO have not been optimized for microwave applications. This thesis will attempt to identify a suitable process for selectively dry-etching high-aspect ratio, high-resolution Ohmic contacts to ZnO devices. The research accomplished in this thesis will provide the foundation upon which further process optimization may result in ZnO TFT X-band operation.

1.3 Assumptions and Limitations

Many methods of achieving good Ohmic contacts to ZnO have been investigated in previous research, as detailed in Section 2.5. However, a few of these methods, namely, pre-Ohmic deposition surface treatment, are not actively pursued research areas at Air Force Research Laboratory (AFRL). ZnO doping will be outside the thesis research scope as well. Furthermore, Ohmic contact formation requiring deposition conditions outside the thermal budget for AFRL ZnO devices (<400°C) are also outside the thesis scope. Therefore, the focus of this research will be identifying materials for selectively etching to ZnO for TFT channel region definition which demonstrate good edge acuity to a patterned mask. Further device optimizations, such as non-critical dimensions, metal alloying and/or annealing, and ZnO thin-film thickness, and fabrication optimizations, such as etch chemistry parameters including gas flow and chamber pressure, photoresist (PR) materials, and other non-critical processing parameters, will also not be pursued in accordance with time constraints placed upon the successfully completing this thesis. Many of these device and fabrication optimizations have been narrowed in scope through previous research at AFRL.

1.4 Methodology

For researching this thesis, an etch study was first executed under a pre-determined etch chemistry for channel definition via electron-beam lithography. The etch study resulted in identifying materials predicted to have high etch selectivity against ZnO. Second, a CD study was conducted applying the etch study results. The CD study allowed

eliminating unsuitable materials and processes for device fabrication through directly observing Ohmic-ZnO material interfaces. Finally, optical and electron beam (e-beam) direct current (DC) device fabrication and testing were accomplished on ZnO devices whose channels were defined with subtractive reactive-ion etching (RIE) in accordance with the results gathered from the CD study. The results from the DC test provide a foundation upon which further device optimization could result in higher ZnO TFT radio frequency (RF) performance than previously reported.

1.5 Summary

The following thesis chapters include a literature review, methodology, results and analysis, and conclusions. The literature review provides a general overview of important information regarding previous research accomplished on ZnO TFTs and provides discussion applying this information in completion of the thesis research. The methodology section applies the information gathered and presented in the literature review to formulate a viable solution for the problem presented. The results and analysis section contains data collected through the methods proposed. Finally, the conclusions chapter summarizes the outcomes and limitations of the research and data presented, and it suggests further research to be accomplished.

II. Literature Review

The Literature Review chapter discusses key material properties and fabrication and design technologies critical to the research contained within this thesis. The first discussion is of the material properties of ZnO, such as its crystal structure, quantum mechanical properties, and electrical properties, necessary for complete understanding of the interest in ZnO transistors. The second section discusses the different methods of ZnO bulk crystal growth. The third section discusses fabrication methods and definitions and their limitations. The fourth and fifth sections contain information regarding device scaling and theory and Ohmic contacts to ZnO, respectively. Each of these sections detail the main purposes behind the research conducted in this thesis and are critical for future applications of the work contained herein.

2.1 ZnO Material Properties

2.1.1 Crystallography

Bulk semiconductor-grade ZnO exists in three different crystal orientations: a cubic rock-salt, a cubic zinc-blende, and a hexagonal wurtzitic structure, the latter being the most common [49] and shown in Figure 2.1 [27]. Hexagonal wurtzite ZnO is characterized as two intersecting sublattices of Zn^{2+} and O^{2-}, resulting in each Zn atom tetrahedrally surrounded by four O atoms, and conversely each O atom tetrahedrally surrounded by four Zn atoms. In this crystallographic orientation, its lattice parameters become $a = 3.2495$Å and $c = 5.2069$Å. Bulk ZnO can therefore be epitaxially grown onto

wurtzitic GaN, whose lattice parameters are a = 3.186Å and c = 5.186Å, and other substrates listed in Section 2.2.2 with minimal crystal lattice strain and interface defects. Other materials on which ZnO has been deposited, including SiO_2 used in this research, are detailed in Section 2.2.2.

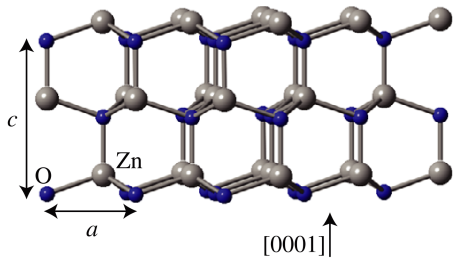

Figure 2.1: Hexagonal wurtzitic crystal structure of ZnO [27]

2.1.2 Electrical Properties

ZnO is a II-VI compound oxide semiconductor with a natural, wide direct bandgap of 3.37 eV at room temperature, yielding low-leakage devices as demonstrated by its large on/off current ratio $>10^{12}$ [2] and allowing light emission in the ultra-violet (UV) region as fabricated LED structures [49]. This bandgap also results in optically transparent devices across the visible light spectrum, with average optical transmittance of 75% and peaks of up to 85% [20, 22]. ZnO has a large exciton binding energy of ~60 meV allowing for room temperature (RT) operation of highly efficient semiconductor diode lasers [69].

ZnO has many interesting properties for electronic device fabrication which set it apart from other single- and compound- semiconductor materials, such as Si and GaN, respectively. For example, ZnO has demonstrated higher radiation-resistance than typical

semiconductor materials such as Si and GaAs [49]. Whereas typical covalently-bonded semiconductors have highly-directional sp-hybrid orbital bonds between their atoms, metal-oxide semiconductor s-orbitals form states near the conduction band minimum. In the presence of high electron energies (≥1.6 MeV) and total radiative flux ($\geq 1 \times 10^{17}$ cm^{-2}), these s-orbitals result in lower electronic transport disruption than when compared to Si, GaAs, CdS, and GaN [52, 80]. Furthermore, these atomic-level effects of radiation have been shown nearly removed after a relatively quick, low-temperature anneal (~200°C) [52, 80]. These particular properties make ZnO devices a potential candidate for space and nuclear applications where radiation is prevalent and thus poses a risk to mission-critical, sensitive electronics.

Undoped ZnO naturally exhibits intrinsic n-type conductivity [21, 22, 27, 49] and very high electron densities have been reported ($\sim 10^{21}$ cm^{-3}) [35]. It is still not entirely understood why undoped ZnO displays this natural n-type conductivity. Some researchers hypothesize that this is due to impurities in the substrate, while others claim a native defect or defects attributes to its conductivity [21, 22, 27]. Within the impurities argument, debate continues over which phenomena are causing this natural doping; it could be low-energy oxygen vacancies or zinc interstitials, or possibly residual copper introduced during the growth process [25, 49]. Other researchers suggest n-type conductivity is solely due to unintentional hydrogen doping acting as a shallow donor in ZnO; some researchers [49] note this argument is valid as hydrogen is always present in all forms of ZnO bulk growth and defuses easily as a result of its large mobility. Further n-type doping has been achieved with various Group-III elements including aluminum, gallium, and indium

[25, 49]. High-quality and highly conductive n-type ZnO films have subsequently been reported by various groups.

Developing bulk p-type ZnO crystal substrates is pursued with the expectation that ZnO would make suitable optoelectronic devices. Unfortunately, suitable p-type conductivity in ZnO has proven difficult to achieve as with most other wide bandgap semiconductors such as GaN and ZnSe [27, 33, 49]. Previous research groups hypothesized p-type conductivity could be achieved with doping known acceptors including Group-V elements, such as N, P, and As, into oxygen vacancies and Group-I elements, such as Li, Na, and K, and Cu and Ag, into zinc vacancies. However, some researchers argue that achieving a shallow acceptor level would be difficult theoretically. Also hypothesized in substituting the aforementioned Group-I elements into Zn sites or Group-V elements into O sites, is the acceptor level would be controlled. Unfortunately, Group-I elements tend to occupy interstitial sites rather than substitute Zn due to their small atomic radii and thus behave as donors. Furthermore, differing bond lengths between Na/K and O introduces lattice strain, which contributes to poor device performance and seminconductor mobility due to quantum well and trap formation. After several reports of successfully growing p-type conductivity ZnO films using various methods and various elements for doping, these channels remain of debatable quality and reliability and are not easily reproducible, and reliable p-n junctions have not been reported [21, 22, 27, 49].

2.2 ZnO Growth

2.2.1 Bulk

ZnO has been grown in its wurtzitic form in bulk by a number of different methods [2, 34, 53], including seeded vapor phase, melt-growth, hydrothermal, and sintering. First proposed by Look, *et al.*, in 1998, seeded vapor phase is a technique in which pure ZnO powder, formed from highly pure Zn vapor and O_2, is heated to 1150°C as H_2 is flowed to transport the vapors to the cooler (1100°C) end of the furnace. At the cooler end, the reaction

$$Zn(g) + H_2O \rightarrow ZnO(s) + H_2(g) \tag{2.1}$$

takes place. ZnO is then formed when the reverse reaction occurs on a single-crystal seed located at the cool end. Using this method for 150 to 175 hours produces 2-inch-diameter crystals 1 cm thick [34]. Melt-growth is a modified Bridgman process [27] involving high-pressure and induction melting via radio frequency (RF) energy, allowing for crystal boule production in sizes up to 5.5 inches in diameter weighing as much as a kilogram [53]. ZnO single crystal samples grown by melt demonstrate high n-type conductivity (10^{17} cm^{-3}) and mobility of $\sim$130$cm^2V^{-1}s^{-1}$ [27, 46, 53]. Hydrothermal growth is accomplished in a low supersaturation environment, utilizing a two-zone furnace from which bulk crystalline ZnO is precipitated onto a single crystal seed within an autoclave [31, 48, 58, 61]. Sintering is a common method for ZnO target manufacturing for pulsed-laser deposition (PLD) thin-film deposition, discussed in Sections 2.2.2 and 3.3.1, whereby high-purity ZnO powder is compressed resulting in high-purity targets [5, 27].

2.2.2 Thin-film

Epitaxial thin-film ZnO growth is accomplished by several methods, including PLD, chemical vapor deposition (CVD), metal-organic CVD (MOCVD), and molecular beam epitaxy (MBE) [27]. Sputtering ZnO techniques generally result in lower quality films from defects introduced via particulate matter during deposition [12, 18]. An important factor in epitaxial growth is substrate lattice-matching to achieve highly crystalline thin-films, necessary for optimal carrier transport and thus device performance. Many suitable substrates have been researched previously, such as sapphire [73], quartz [72], glass [17, 75, 78, 81], α-Al_2O_3 [35, 57, 77], GaAs [24, 55–57], CaF_2, $ScAlMgO_4$ (SCAM) [70], Si [77], and GaN [26]. Of these, ZnO grown via PLD on SCAM is notable due to its extremely low 0.09% lattice mismatch resulting in high quality crystalline structures, minimal defects, and high reported mobility of $440 cm^2 V^{-1} s^{-1}$ [27, 70]. The MBE growth regime has few studies reported since the first in 1996 [27]. The MOCVD growth regime is regarded as ideal for laser and light-emitting diodes (LEDs) and solar cells [27].

The ZnO thin-films to be used throughout this research are grown via PLD. Their growth parameters are discussed in Section 3.3.1.

2.3 Fabrication Methods and Definitions

2.3.1 Lithography and Pattern Transfer Techniques

In device design and fabrication, photoresist (PR) is a light-sensitive polymer commonly used for patterning device structures. Its material properties are modified when exposed to light and are categorized into either positive or negative types. With positive

PRs, the polymer bonds decompose when exposed to light and the material becomes more easily soluble when certain chemicals are applied, called developers. Likewise, negative PRs bonds are strengthened when exposed to light. The PR used throughout the thesis research was positive. Certain types of PRs respond to different wavelengths of light. For example, the 1800 series PR responds well to UV light while acting as a mask under deep ultra-violet (DUV). Furthermore, most polydimethylglutarimide (PMGI) PRs, such as the SF-series, react under DUV exposure instead of UV. A third type of PR reacts to high-energy electron bombardment resulting in feature sizes better than 0.1μm. This PR is referred to as electron beam (e-beam) photoresist, and a few common examples include poly-methyl methacrylate (PMMA), poly-butene-1 sulfone (PBS), and ZEP-520a [30, 37, 38, 45, 51].

Traditional contact photolithography techniques involving UV or DUV are limited in feature size due to the material limitations of the PRs used during processing, while offering high-resolution patterning from its 1:1 mask pattern transfer. One application of PR is patterning etch areas in removing unnecessary material through wet or dry etching, where the patterned PR acts as an etchant block. Another application of PR is metal lift-off, in which a pattern is transferred from a mask to a double-stack of PR through UV and DUV and developing. When the sample is exposed to metal evaporation, a highly directional method of metal deposition, the open areas of the pattern will remain when the metal is removed, or "lifted off," with the top PR layer. The bottom PR layer is removed leaving the protected channel exposed. A simple method of removing the unwanted metal is by using adhesive tape. In defining a thin-film transistor (TFT) channel, metal is

deposited in the pattern of the device while the channel area is blocked with PR, and then removed. The subsequent device has a channel with the dimensions of the PR. However, if the PR pattern is too narrow with respect to its thickness, the internal PR stress causes it to lose adhesion to the surface and warp. In extreme cases, the PR could develop entirely leaving an open region where the channel should be protected. Hence, optical lithography can maintain its structural integrity only to certain device dimensions before other methods must be used. Furthermore, contact optical lithography can only pattern features in resolutions larger than the wavelength λ of the UV used for exposure. The Karl Suss MA6 Mask Aligner at Air Force Research Laboratory (AFRL) has λ = 365-405nm and thus limits mask feature sizes for contact lithography to those dimensions.
[30, 37, 38, 45, 51].

In e-beam lithography, special PR designed to decompose under a focused beam of electrons is used to achieve very small dimensions. The e-beam tool operates not unlike the scanning electron microscope (SEM) tool, where electrons generated by a gun are guided through a column of condenser lenses and steered in a pre-defined pattern. The spot size at the sample's surface where the electrons converge can be on the order of several nm in diameter allowing for fine features to be fabricated through the developed e-beam PR. A limitation of SEM tools also exists with e-beam tools, where the scan field is typically much smaller than the sample being exposed, or written. A precision mechanical stage guides the sample to a new location for the e-beam to continue patterning the remainder of the sample. If the stage is not moved precisely, stitching can occur where written reticules will become misaligned with their neighbors [37, 54].

Contact photolithography and e-beam lithography are the two most commonly used methods of device patterning available at AFRL. In addition to e-beam lithography to achieve < 1μm channel lengths, other methods exist in other research groups and in mass-production environments. These methods require specialized tools and include immersion optical lithography, stepper, Extreme UV (EUV), X-ray lithography, and ion beam lithography [37]. However, except in the case of a stepper which will not be used for this research, these patterning methods are not available at AFRL. To achieve the smallest device channel dimensions for reasons explained in Section 2.4, e-beam lithography will be chosen over traditional optical.

2.3.2 Etching

Several material etching methods are available for device fabrication and processing at AFRL. In device fabrication, etching is generally categorized into two types: wet and dry. Wet etching requires using acids and is more applicable to large-feature fabrication due to its fast etch rates (ERs) resulting in surface abrasion and undercutting, particularly with ZnO. Dry etching can be accomplished with a plasma-assisted etch (PAE) systems, such as reactive-ion etching (RIE), deep reactive-ion etching (DRIE), or inductively-coupled plasma (ICP). Generally, this method of etching is optimized for high-aspect-ratio, anisotropic structural fabrication at the expense of surface damage. However, modifications can be made such that the chemical etching component in a PAE system is enhanced achieving isotropic etch profiles.

Device channel scaling is more easily accomplished using subtractive etching methods defined by small lithography features or through lifting off a metal pattern

leaving a channel defined on the device. However, wet etching proves difficult to control at the smallest device features, particularly nano-scale channel dimensions. ZnO has a strong reactivity to acids and therefore lateral dimension control is compromised [71]. The lift-off method of channel definition is limited to large dimensions due to optical lithography limitations. Dry etching provides a unique opportunity for achieving small device dimensions through subtractive etch processing. However, to be most beneficial against the other channel definition methods, a PAE must perform an "etch-stop" on the ZnO; that is, leaving the ZnO top surface either unscathed or in an easily-recoverable state. A material which etches quickly compared to ZnO etching slowly under a particular PAE chemistry is necessary, and this ratio is termed "etch selectivity." A PAE of a material with high selectivity ratio to ZnO will effectively achieve an etch-stop. However, to reduce the top surface damage to ZnO, the etch rate of ZnO under this chemistry must also be low.

One PAE example is RIE. Similar in design to the plasma system shown in Figure 2.2 [50], the bottom electrode on which the sample resides is also connected to the RF power supply. Etch gases are flowed into a chamber at vacuum pressure until a stable chamber pressure is reached, then a plasma is ignited [50]. By connecting the bottom electrode to the RF power supply, an enhancement of the physical etching component through increased ion energy incident upon the sample is achieved [50]. Therefore, both chemical reaction and physical ion components are available and important in this etching system [50]. The RIE system has a stronger ion impact than a simple plasma system, resulting in a more physical and directional etch [50]. In a subtractive etch process for device scaling, a directional etch will be important in achieving vertical sidewall profiles

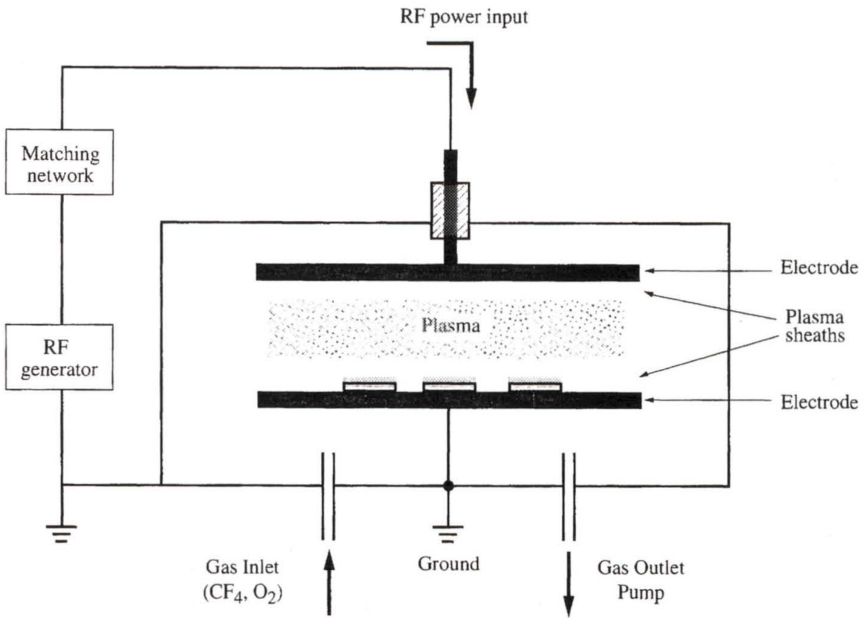

Figure 2.2: RF Plasma Etch System Schematic [50]

allowing source-drain spacing reduction to sub-micron dimensions. A reduction in platen RF power would therefore be expected to reduce the physical etching effect, and correspondingly the chemical reaction component would become dominant thus increasing isotropy. However, RIE could possibly cause surface radiation, damage to the crystal lattice, and surface charge buildup, and the increased physical etching component reduces selectivity [50]. Each of these effects will have a detrimental impact on developing a highly-selective, subtractive etch process, and thus RIE tool parameters, such as gas flow, platen power, direct current (DC) bias, and chamber pressure, must be optimized to achieve those desired results.

2.4 Device Theory and Scaling

Device scaling is used to achieve improved device performance characteristics. Among these, transistor size reduction, increased I_{ds} per mm channel width, power supply voltage reduction, and load capacitance reduction are a few of the common goals in some research groups [43]. However, with device scaling arrives challenges which must be addressed including maintaining an adequate I_{on}/I_{off} ratio and correspondingly a low leakage current, controlling the short-channel effects, and maintaining a stable driving current [43]. The goals for ZnO devices being researched at AFRL include RF performance, high power, and even switching [1–4].

In the case of a normally off, n-channel MOSFET (NMOS) transistor, electrons are depleted in the channel region until a gate voltage bias V_{gs} nearing the device's threshold voltage V_t is applied and accumulation forms. As V_{gs} increases such that $V_{gs} \geq V_t$, an inversion channel of electrons is formed and conduction occurs. Saturation occurs when the channel can no longer support an increase in current. High-frequency devices switch in the saturation region, in which the drain current I_{ds} can be described by [60]

$$I_{ds} = K\left(V_{gs} - V_t\right)^2 (1 + \lambda V_{ds}) \tag{2.2}$$

given [60]

$$K = \frac{1}{2}\mu_n c_g \left(\frac{W_c}{L_c}\right), \tag{2.3}$$

where μ_n is mobility, c_g is gate capacitance per unit area, W_c is channel width, L_c is channel length, and λ is a positive, constant metal-oxide-semiconductor field-effect transistor (MOSFET) design parameter related to the Early voltage. Mobility can be

increased through doping or ZnO deposition parameter modifications which results in higher current for a given charge concentration. However, mobility enhancement is outside the thesis scope as a standard ZnO deposition recipe has been previously determined at AFRL [4]. An alternative to mobility enhancement in achieving increased I_{ds} is reducing the distance electrons travel from the source to drain. The distance an electron travels between the source and drain is defined by the channel length L_c. Therefore, to increase I_{ds}, device scaling is utilized in reducing L_c. Furthermore, it has been shown [3] that logarithmic L_c scaling of ZnO devices results in a corresponding logarithmic scaling of current density, allowing for accurate predictions of future device design performance.

The transconductance g_m of a MOSFET is described by [36]

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}. \tag{2.4}$$

When Equations (2.2) and (2.4) are combined and assuming an ideal transistor ($\lambda = 0$), the transconductance of a MOSFET in the saturation region is derived to be

$$g_m = 2K\left(V_{gs} - V_t\right) = \mu_n c_g \frac{W_c}{L_c}\left(V_{gs} - V_t\right). \tag{2.5}$$

From Equations (2.3) and (2.2), drain current I_{ds} is proportional to (W_c/L_c). Therefore, as the gate length decreases, the drain current increases. Likewise, the transconductance increases with a decrease in gate length.

As L_c becomes smaller, the channel length variation after lithography and development will have a larger impact on I_{ds}. For example, given a certain transistor with $L_c = 1\mu\text{m}$, $I_{ds} = 10\text{mA}$, and holding all other variables constant at $x = L_c \times I_{ds} = 10^{-8}$

A·m, if $\Delta L_c = \pm 5\% \implies L_c' = L_c(1 \pm 0.05)$, then

$$I_{ds} = \frac{x}{L_c'} = \frac{10^{-8}}{(1 \pm 0.05) \times 10^{-6}} \implies 9.52\text{mA} < I_{ds} < 10.52\text{mA}, \tag{2.6}$$

and the drain current across multiple devices with the same nominal L_c will vary by 1mA. If L_c is reduced to 100nm and $\Delta L_c = \pm 5\%$, while other device parameters remain constant, then

$$I_{ds} = \frac{x}{L_c'} = \frac{10^{-8}}{(1 \pm 0.05) \times 10^{-7}} \implies 95.2\text{mA} < I_{ds} < 105.2\text{mA}, \tag{2.7}$$

and the drain current across multiple devices with the same nominal L_c will vary by 10mA, which is significantly higher. As channel dimensions scale, variation produces significantly larger effects in electrical characteristics that affect modeling, and thus introduce difficulties in designing circuits such as RF amplifiers. Therefore, it is critical channel length dimensions are well-controlled and repeatable to minimize ΔL_c. A method of repeatably defining device critical dimensions (CDs) is with e-beam lithography, which also enables smaller features than typical contact optical lithography. Furthermore, materials must be selected for subtractive channel definition in which the etch process is well-controlled and repeatable. Etch processes which result in under-cutting, result in material redeposition, and/or exhibit poor edge acuity (follow the PR profile) are not well-controlled or repeatable.

The unity current gain frequency f_t at which the common-source current gain $|h_{21}| = I_{out}/I_{in}$ becomes unity [60] is described by Equation (2.8) [14].

$$\frac{2\pi}{f_t} = \tau = \frac{c_g}{g_m} \implies f_t = \frac{g_m}{2\pi c_g} \tag{2.8}$$

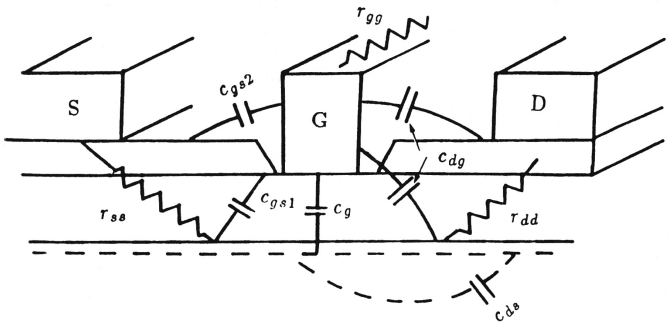

Figure 2.3: HEMT Structure with Parasitic Resistances and Capacitances [13]

During high-frequency operation, if V_{gs} modulation is greater than f_t, the output I_{ds} will be attenuated. As f_t is dependent upon g_m, the conclusion can be drawn that while channel length decreases f_t will increase. However, these equations are applicable for an ideal transistor model only. When considering parasitic resistance and capacitance components, shown in Figure 2.3, source resistance r_{ss} directly impacts transconductance [13]

$$g'_m = \frac{g_m}{1 + g_m r_{ss}} \tag{2.9}$$

where g'_m is effective transconductance. The g'_m replaces g_m in the previous equations. It is therefore important to keep r_{ss} as low as possible to minimize the impact on g_m, f_t, and I_{ds}.

2.5 Ohmic Contacts to ZnO

When a metal is brought into intimate contact with a semiconductor, electron transfer between the materials occurs until a thermal equilibrium is formed. The electrons transferred and their direction is dependent upon the metal and semiconductor work functions (Φ_{M} and Φ_{SC}, respectively) and the electron affinity (X_{SC}) of the semiconductor [36]. Multiple types of metal-semiconductor contacts arise imparted by each material's

initial conditions, the outcomes of which are detailed in Figure 2.4 [6]. For the work contained in this thesis, the ZnO semiconductor is n-type and therefore only Figures 2.4a and 2.4b are applicable. The Schottky barrier of the thermal equilibrium for an n-type semiconductor, (Φ_{SB}), is governed by the simple Schottky model, duplicated in Equation (2.10) [43, 68].

$$q\Phi_{SB} = q(\Phi_M - X_{SC}) \tag{2.10}$$

A Schottky or rectifying contact is formed when $\Phi_{SC} < \Phi_M$, creating a high-resistance barrier for small applied V_{DS} under reverse bias conditions. Ideally, Φ_{SB} should be near 0 eV to form an Ohmic (non-rectifying) contact [7]. Thus, Φ_{SC} must be nearly equivalent to or larger than Φ_M allowing carriers to flow freely between the contact and semiconductor in both directions.

Experimentally, a typical II-VI compound semiconductor exhibits ionic bonding, unpinned Fermi energy levels, and have shown Φ_{SB} to be strongly dependent on Φ_M [7]. Contrarily, covalent semiconductors, including most III-V compounds, contact with metals tend to have a Φ_{SB} independent of Φ_M [7, 40], due to a substantial Fermi pinning in the bandgap [6, 7, 39, 67]. ZnO, a II-VI compound, borders both ionic and covalent semiconductors and thus allows for low resistivity Ohmic contact formation through a combination of barrier height reduction and/or doping [7]. Decreasing the barrier height allows for higher thermonic emission and thus lower resistivity. Doping allows a thinner barrier width and thus increased carrier tunneling from field emission [7]. However, ZnO doping is not within the thesis scope. Materials with work functions similar to that of ZnO

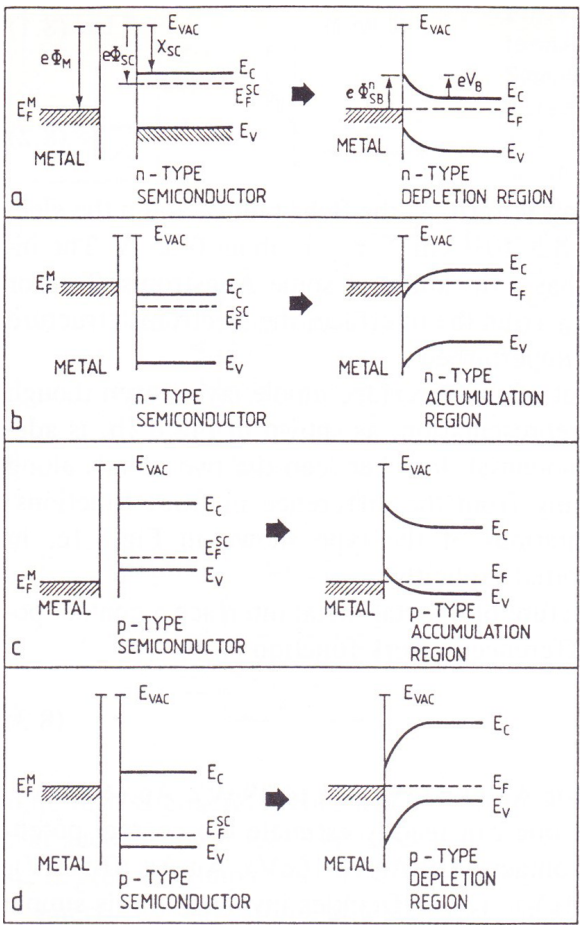

Figure 2.4: Band Diagrams Before and After Metal-Semiconductor Contact [6]

(X_{ZnO}~4.2eV [7]) and low conductivity allow for thinner layers to be deposited. As thinner layers are utilized, alternative PRs with the ability to maintain structural integrity during RIE despite their quicker etch rates become available. Furthermore, thinner layers require less etch time resulting in better etch profiles from lateral PR etch rate reduction. Smaller gate geometries can be obtained with thinner contact layers because surface morphology is minimized, allowing for clean lithography through reducing back-scattered UV light or electrons.

Ohmic contacts have been demonstrated as necessary device access materials for a wide variety of ZnO devices [7]. Both Ti [39, 76] and Au [16, 39, 42] have been demonstrated to make Ohmic contacts to ZnO [7]. Many other materials have been discovered to form Ohmic contacts with ZnO. Brillson, *et al*, compiled a list of several of these materials from various resources [7]. This list has been duplicated in Table 2.1 with their corresponding original citations, less the non-ideal formation schemes. Non-ideal formation schemes include those which required an annealing condition outside of the AFRL ZnO thermal budget (>400°C), those with p-type ZnO carrier concentration, and those with the higher ρ_c amongst their same-material counterparts. Some research groups have demonstrated reduced ρ_c through plasma surface treatments before depositing Ohmic contact material [32, 47]. Lee, *et al.*, reported as-grown, Ar plasma treated, and H_2 plasma treated Ti/Au contacts to ZnO with $\rho_c = 7.3 \times 10^{-3}$, 5.0×10^{-4}, and 4.3×10^{-5} Ω-cm^2, respectively [32]. Oh, *et al.*, used KrF laser irradiation in N_2 and O_2 ambient gases to obtain Ti/Au contacts to ZnO with $\rho_c = 3.22 \times 10^{-4}$ and 1.82×10^{-4}, respectively [47].

While RF performance with mesa-isolated, $L_g = 1.2$μm ZnO devices has been demonstrated by Bayraktaroglu, *et al*, using a Ti/Pt/Au metal stack [2], further device optimization resulting in a higher f_t can be obtained through device scaling [13, 14, 43] and identifying other Ohmic contacts using commonly available sputtering materials at AFRL. Commonly available materials for sputtering and evaporation at AFRL where the research in this thesis will be conducted include molybdenum, tantalum, titanium tungsten (alloy, 10% titanium to 90% tungsten, or simply “10-90”) and tungsten. The availability of these metals at AFRL for sputtering reduces the time required to deposit these

Table 2.1: Ohmic Contacts to ZnO

Metal	ZnO n (cm^{-3})	Anneal. Cond.	ρ_c (Ω-cm^2)	Reference
Al/Au	1×10^{17}	None	2.5×10^{-5}	[62]
Al/Pt	2×10^{18}	None	1.5×10^{-5}	[28]
Ta/Au	1×10^{17}	300°C/N_2/30 sec	5.4×10^{-6}	[63]
Ti/Al	1.7×10^{18}	300°C/N_2/1 min	9.7×10^{-7}	[29]
Ti/Al/Au	(n)	None	4.1×10^{-5}	[44]
Ti/Al/Pt/Au	(n)	None	4.2×10^{-5}	[44]
Ti/Au	2×10^{17}	None	4.3×10^{-5}	[32]
Ti/Au	(n)	None	4.2×10^{-5}	[44]
Ti/Au	1.9×10^{19}	None	2.4×10^{-7}	[10]
Ti/Au	1.9×10^{19}	300°C/O_2/1 min	6×10^{-8}	[10]
Ti/Pt/Au	(n)	None	4.8×10^{-5}	[44]

materials, which assists in meeting the thesis timeline. The resistivity (ρ) and work function (Φ_M) of these sputtered metals at AFRL have been widely reported. Each material has important properties which can vary depending on deposition parameters and growth conditions. Under the experiment conditions, where annealing to ZnO is not accomplished and substrate is RT during deposition, the values of these material properties are listed in Table 2.2, along with their corresponding references.

Table 2.2: Resistivity and Work Function of Target Materials at RT

Material	ρ (Ω-cm)	ρ Ref.	Φ_M (eV)	Φ_M Ref.
Mo	10-15$\times 10^{-5}$	[59]	4.94 (bcc)	[66]
nc-Si	2.8×10^{-2}	Measured	-	-
Ta	2.1×10^{-4}	[74]	5.08 (bcc)	[66]
TiW (10-90)	$\sim 7.2 \times 10^{-5}$	[19]	-	-
W	2.4×10^{-5}	[64]	5.62 (bcc)	[66]

Additionally, a new semiconductor-semiconductor contact interface to ZnO which has been previously unreported using nanocrystalline silicon (nc-Si) will be studied in this thesis. Studying nc-Si-ZnO contacts will allow comparisons to be made regarding etch profiles, etched surface damage, CDs, and other important device performance characteristics of the metal-ZnO interfaces listed above. The ρ was calculated through the efforts of AFRL engineers prior to data collection and is also reported in Table 2.2. The work function Φ_{SC} of nc-Si varies by material growth parameters [79]. The Φ_{SB} of all materials in Table 2.2 is currently unknown when brought into intimate contact with ZnO. The nc-Si to be studied in this thesis will be provided by the University of Toledo. The deposition and growth parameters of nc-Si is detailed in Section 3.3.2.2.

2.6 Summary

This chapter presented information vital to successful thesis research. Many design considerations must be factored into the devices fabricated in Chapter 3 for successfully

completing the thesis research. Contact materials deposited onto ZnO must be Ohmic in nature while also meeting the criteria of being readily available for fabrication at AFRL, subtractively and selectively etched against ZnO, etched in a high-aspect-ratio manner, and etched with good edge acuity to the PR profile to achieve small CDs.

III. Methodology

THE Methodology chapter discusses the various methods data was gathered and interpreted in completing the research. Throughout the remainder of the thesis document, many chemical elements are presented in their abbreviated form. A list of all chemical elements presented in this thesis can be found in Appendix A. An introduction section outlines the device and design concepts utilized throughout data collection. The next section lists all materials selected and their growth techniques and/or processing parameters. An etch study was executed resulting in the first set of data collected. Applying the results of the etch study, a critical dimension (CD) study was accomplished for observing device layer structure and photoresist (PR) edge acuity. The CD study resulted in eliminating non-ideal fabrication steps for channel scaling applications. Finally, optically-defined and electron beam (e-beam)-defined subtractive etch devices were fabricated and tested for their direct current (DC) performance.

3.1 Introduction

The Air Force Research Laboratory (AFRL), Sensor Directorate, has developed a maskset capable of fabricating fully-functional radio frequency (RF) ZnO thin-film transistor (TFT) monolithic microwave integrated circuits (MMICs). A subset of this maskset is called the QuickLot process. The QuickLot process allows for rapid material and device process analysis and development. Contact resistance and layers, growth conditions, mobility, and other important experimental device fabrication information can

be obtained from the QuickLot process with minimal fabrication. The QuickLot process contains transmission line model (TLM) structures for determining contact sheet resistance ρ_s. The devices fabricated throughout this thesis are based on the QuickLot process for rapid device fabrication and procedural analysis. Section 3.6 and Figure 3.4 provide further QuickLot design details. The processing steps listed in this chapter were executed in a Class 100 cleanroom.

3.2 Etch Chemistry

It was previously observed at AFRL that the standard SiO_2 reactive-ion etching (RIE) chemistry does not appear to etch ZnO. The standard SiO_2 RIE chemistry used at AFRL is an anisotropic etch, composed of CF_4 and O_2 with a flow rate of 40 sccm and 3 sccm, respectively, at 40 mTorr chamber pressure and 200W platen power. For experimental simplicity, these gas ratios and pressure remained constant throughout the thesis research. Four target RIE powers were selected for study: 200, 150, 100, and 50W. The DC bias was dependent on the RF power, loading, and reflective power, each of which varied with sample material composition and size. The tool used for RIE etching was a Unaxis 790 series RIE.

3.3 Materials Overview

3.3.1 Zinc Oxide

The ZnO films thin-films used throughout this thesis were deposited by pulsed-laser deposition (PLD) at AFRL. The PLD system used was a Neocera Pioneer 180, with a KrF excimer laser (λ = 248 nm) at 30 Hz with a 10 ns pulse duration at an energy density of

2.6 J/cm^2. The base chamber pressure was 1×10^{-7} Torr with 10 mTorr O_2 partial pressure throughout deposition. The ZnO thin-films were deposited at 200°C. The 76.2 mm diameter p-type Si substrate with 25nm SiO_2 isolation layer was rotated at 20°/sec while the ZnO target was rotated at 40°/sec, raster velocity of ±2° at 5°/sec. The distance from the target to the substrate was 9.5 cm and shifted by approximately 5 cm off the rotation axis. The target was a sintered ZnO ceramic disk (99.999%) measuring 50 mm in diameter and 6 mm thick. Laser raster velocity with an inverse velocity profile was accomplished through laser focusing optics mounted to and controlled by a programmable traveling optical train mechanism. This inverse velocity profile results in a constant laser footprint size on the target throughout its scanning speed range. These parameters combined yielded a film with 8% variation in thickness on the substrate.

Following deposition by PLD, the ZnO thin-film was annealed in atmosphere air at 400°C for 1 hour. This annealing process is a standard device fabrication step at AFRL. The deposition temperature and bake temperature and time resulted from a design of experiments in an attempt to identify the optimal grain size resulting in the highest current density of ZnO semiconductor for best device performance [4].

3.3.2 Contact Materials

Many materials were selected for observation and testing based upon their electrical properties and growth characteristics. In particular, materials deposited on ZnO must be accomplished within the thermal budget (<400°C) so as not to increase the grain size of the nanocrystalline ZnO layer. A modified grain structure from previous research would have adverse affects on device performance, including a lower on-off current ratio and

lower turn-on voltage. The materials selected for deposition on ZnO were also chosen for their low resistivity (ρ).

3.3.2.1 Molybdenum

Molybdenum (Mo) is a material readily available at AFRL and is known to etch in CF_4 gas. It was thus selected as a target material to contact and subtractively etch against ZnO. The Mo thin-films used throughout this thesis were prepared with the sputter-deposition method. The sputtering tool used was a Denton Discovery 18 Sputtering System. The power was 275 W. The inert gas used was Ar at a flow rate of 75.8 sccm, resulting in a chamber pressure of 4.0 mTorr. The metal was sputtered for 165 seconds to achieve a Mo thin-film 1000Å nominal thickness, resulting in a deposition rate of 6.06 Å/sec. This deposition process was executed on an n-type Si 1-10 Ω-cm wafer for the etch study and 50 or 75nm of ZnO grown by PLD for the etch and CD studies and device fabrication.

3.3.2.2 Nanocrystalline Silicon

The nanocrystalline silicon (nc-Si) thin-films used throughout this thesis were grown by the University of Toledo. The nc-Si was chosen for its known reactivity in the SiO_2 RIE chemistry, and low deposition temperature (<400°C). The nc-Si was deposited via plasma-enhanced chemical vapor deposition (PECVD), with substrate temperature T_s = 200°C, the total pressure p = 1.5 Torr, the plasma power density P = 0.032 W/cm^2, the hydrogen dilution ratio $R = [H_2]/[SiH_4] = 100$, and the doping gas ratio $D = [PH_3]/[SiH_4] = 0.0125$ each held constant throughout deposition. The nc-Si films

were monitored with real time spectroscopic ellipsometry (RTSE) throughout deposition [9].

3.3.2.3 Tantalum

Tantalum (Ta) is a material readily available at AFRL and is known to etch in CF_4 gas. It was thus selected as a target material to contact and subtractively etch against ZnO. The Ta thin-films used throughout this thesis were prepared with the sputter-deposition method. The sputtering tool used was a Denton Discovery 18 Sputtering System. The power was 300W. The inert gas used was Ar at a flow rate of 75.8 sccm, resulting in a chamber pressure of 4.0 mTorr. The metal was sputtered for 196 seconds to achieve a Ta thin-film 1000Å nominal thickness, resulting in a deposition rate of 5.09Å/sec. This deposition process was executed on an n-type Si 1-10 Ω-cm wafer for the etch study and 50 or 75nm of ZnO grown by PLD for the etch and CD studies and device fabrication.

3.3.2.4 Titanium Tungsten

Titanium tungsten (TiW) (10:90 alloy) is a material readily available at AFRL and is known to etch in CF_4 gas. It was thus selected as a target material to contact and subtractively etch against ZnO. The TiW alloy thin-films used throughout this thesis were prepared with the sputter-deposition method. The ratio of Ti to W was 10:90 and remained constant throughout the research. The sputtering tool used was a Denton Discovery 18 Sputtering System. The power was 250W. The inert gas used was Ar at a flow rate of 75.8 sccm, resulting in a chamber pressure of 4.0 mTorr. The metal was sputtered for 270 seconds to achieve a TiW thin-film 1000Å nominal thickness, resulting in a deposition rate of 3.70Å/sec. This deposition process was executed on an n-type Si

1-10 Ω-cm wafer for the etch study and 50 or 75nm of ZnO grown by PLD for the etch and CD studies and device fabrication.

3.3.2.5 Tungsten

Tungsten (W) is a material readily available at AFRL and is known to etch in CF_4 gas. It was thus selected as a target material to contact and subtractively etch against ZnO. The tungsten thin-films used throughout this thesis were prepared with the sputter-deposition method. The sputtering tool used was a Denton Discovery 18 Sputtering System. The power was 250W. The inert gas used was Ar at a flow rate of 75.8 sccm, resulting in a chamber pressure of 4.0 mTorr. The metal was sputtered for 230 seconds to achieve a W film 1000Å nominal thickness, resulting in a deposition rate of 4.34Å/sec. This deposition process was executed on an n-type Si 1-10 Ω-cm wafer for the etch study and 50 or 75nm of ZnO grown by PLD for the etch and CD studies and device fabrication.

3.4 Etch Study

To perform an etch-stop on ZnO for subtractive channel definition, the material being etched must have a substantially high etch ratio. The etch ratio is defined as the etch rate of the contact material to the etch rate of the ZnO, and is therefore a dimensionless unit (d.u.). A high selectivity ratio is instrumental in minimizing the degrading of the active channel layer and thus device performance. An effective selectivity ratio between contact materials and the ZnO active channel layer was established through an etch study.

3.4.1 Zinc Oxide

ZnO was previously known to be difficult to etch under the SiO_2 RIE chemistry. The ZnO samples were prepared as outlined in Section 3.3.1.

3.4.2 Contact Materials

The materials listed in Section 3.3.2 were tested for their etch rates under the SiO_2 etch chemistry. Each material was deposited on individual 3" n-type Si 1-10Ω-cm substrates. Unless otherwise noted, all etch materials were scored into 1.5×1.5 cm^2 samples and masked with a mechanical mask composed of n-type Si 1-10Ω-cm secured with Capton tape. The mechanical mask established the etch boundary and, being thicker than PR, allowed for longer etch times where PR may be consumed. Etch rates were calculated by measuring the step height at the etch boundary using a profilometer divided by the etch time.

An example of a profilometer step height, taken from the ZnO with Ni mask sample (detailed in Section 4.2.1), is shown in Figure 3.1. All profilometer measurements were captured with a KLA Tencor P-16+, at a scan speed of 20 μm/s, sampling rate of 200 Hz, force of 1 mg, range of 13 μm, and resolution of 0.0078Å. The profilometer was calibrated before and verified after measuring sessions with a 440Å calibration standard to ensure accurate step height measurements throughout data collection. The profilometer noise is important to note in Figure 3.1, as step heights must be generated so as not to be masked by the noise. Etched sample step heights were targeted to >500Å; samples which measured less than this were discarded and a new sample with the same etch parameters etched at a longer time.

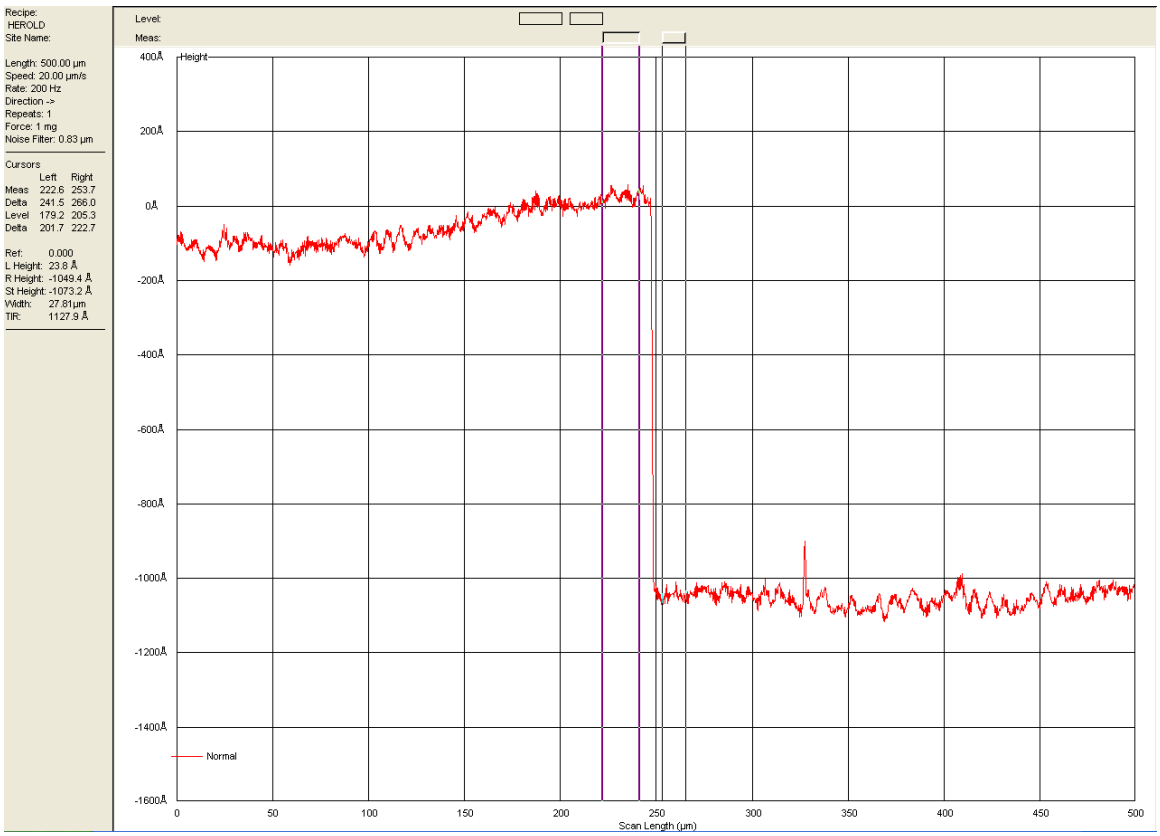

Figure 3.1: Profilometer Data Example

3.4.3 Photoresist

Determining the etch rate of PR utilized for device fabrication is necessary to ensure mask integrity during critical etching operations with the RIE tool. The etch rate of PR can vary dependent upon the material(s) underneath it. To calculate a general PR etch rate, the step height of the PR was recorded before etching patterned devices d_{resist}, measured again after etching for time t resulting in a combined step height of the etched PR and masked material d_{etched}, and finally the etched PR removed and measuring the step height of the masked material by itself $d_{material}$. The PR etch rate can then be calculated from

Equation (3.1):

$$\frac{d_{resist} - d_{etched} - d_{material}}{t} \tag{3.1}$$

An average from different patterned materials was calculated at each RIE power to estimate the PR etch rate.

Due to its material expense and time-consuming processing, the ZEP-520A PR etch rate used for e-beam lithography was calculated differently from typical optical lithography PRs. A small sample of ZEP on a 2" silicon wafer was provided. The sample was scored into pieces and masked with a mechanical mask composed of n-type Si 1-10Ω-cm secured with Capton tape. The mechanical mask established the etch boundary. The ZEP etch rates were then calculated by measuring the step height at the etch boundary using a profilometer as detailed in Section 3.4.2.

3.5 Critical Dimension Study

Good contact definition demands high-aspect ratio etches with good edge acuity and minimized undercut. Therefore, the next phase of research characterized the etch profile of the SiO_2 etch chemistry and materials with regards to aspect ratio and undercutting in a CD study. The results of the etch study from Section 3.4 were applied for preliminary patterning for observing the contact-ZnO interface layer and etch edge acuity and profile. A Karl Suss MA6 Mask Aligner was used throughout this section for PR patterning. More information regarding the mask patterns used in the CD study are provided in Section 3.6. A Hitachi SU-70 and FEI Strata DB235 were used for scanning electron microscope (SEM) and focused ion beam (FIB) imaging and milling, respectively,

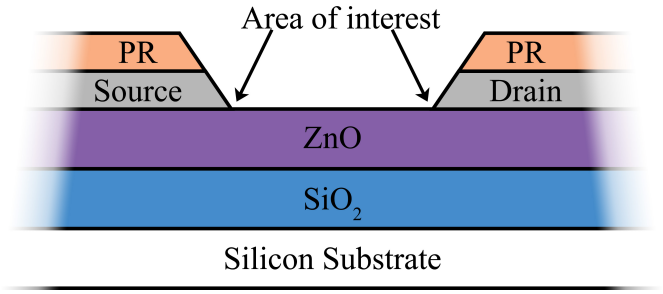

Figure 3.2: Etch Profile Area of Interest (not to scale)

throughout the CD study. The DB235 uses a gallium ion beam for FIB milling and deposits platinum to reduce the curtaining effect. The etch profile area of interest in observing the aspect ratio and edge acuity for contact materials is shown in Figure 3.2.

3.5.1 Molybdenum

The wafer used for the molybdenum CD study was a 3" p-type conductive substrate with 25nm SiO_2 grown via PECVD and 75nm ZnO grown via PLD as discussed in Section 3.3.1. The ZnO was not post-deposition baked. Molybdenum was sputtered as discussed in Section 3.3.2.1 at 1000Å thick. A layer of polydimethylglutarimide (PMGI) SF-11 PR was spun on the wafer at 4000 rpm for 30 seconds at a ramp of 200 rpm and baked for 10 minutes at 250°C. A second PR layer of 1805 was spun on the wafer at 4000 rpm for 30 seconds at a ramp of 200 rpm and baked for 75 seconds at 110°C. Using the Ohmic mask from the QuickLot process, the PR was exposed for 1.9 seconds on the MA6 mask aligner (10mW/cm^2, λ = 365-405 nm), developed with 1:5 ratio of 351 and deionized water (DI) at 500 rpm for 30 seconds, rinsed with DI at 500 rpm for 30 seconds, and dried with N_2. The SF-11 was then exposed to deep ultra-violet (DUV) for 200

seconds with the 1805 acting as the mask, developed with 101 developer for 120 seconds, rinsed in DI, and dried with N_2. The sample was scored into several pieces for multiple SiO_2 RIE chemistry tests observing the features listed above in the introduction of Section 3.5. The samples were submitted to SEM imaging for FIB cross-sectioning for structural layer observation.

3.5.2 Nanocrystalline Silicon

A p-type Si substrate wafer with 1160Å of nc-Si on 1000Å of SiO_2 was provided by the University of Toledo. 1813 PR was spun on at 4000 rpm for 30 seconds at a ramp of 200 rpm and baked for 75 seconds at 110°C. Using the Ohmic mask from the QuickLot process, the PR was exposed for 5 seconds on the MA6 mask aligner (10mW/cm^2, λ = 365-405 nm), developed with 1:5 ratio of 351:DI at 500 rpm for 30 seconds, rinsed with DI at 500 rpm for 30 seconds, and dried with N_2. The sample was scored into four pieces, representing the independent RIE power levels used throughout research. Using the material thickness information provided by the University of Toledo and the nc-Si etch rate calculated in Section 3.3.2.2, a 15% over-etch time was calculated at each power level and the respective samples etched in the RIE 790 tool. Each sample was submitted to SEM imaging for FIB cross-sectioning for structural layer observation.

3.5.3 Tantalum

The wafer used for the tantalum CD study was a 3” p-type conductive substrate with 25nm SiO_2 grown via PECVD and 75nm ZnO grown via PLD as discussed in Section 3.3.1. The ZnO was not post-deposition baked. Tantalum was sputtered as discussed in Section 3.3.2.3 at 1000Å thick. A layer of PMGI SF-11 PR was spun on the

wafer at 4000 rpm for 30 seconds at a ramp of 200 rpm and baked for 10 minutes at 250°C. A second PR layer of 1805 was spun on the wafer at 4000 rpm for 30 seconds at a ramp of 200 rpm and baked for 75 seconds at 110°C. Using the Ohmic mask from the QuickLot process, the PR was exposed for 1.9 seconds on the MA6 mask aligner ($10mW/cm^2$, λ = 365-405 nm), developed with 1:5 ratio of 351:DI at 500 rpm for 30 seconds, rinsed with DI at 500 rpm for 30 seconds, and dried with N_2. The SF-11 was then exposed to DUV for 200 seconds with the 1805 acting as the mask, developed with 101 developer for 120 seconds, rinsed in DI, and dried with N_2. The sample was scored into several pieces for multiple SiO_2 RIE chemistry tests observing the features listed above in the introduction of Section 3.5. The samples were submitted to SEM imaging for FIB cross-sectioning for structural layer observation.

3.5.4 Titanium Tungsten

The wafer used for the titanium tungsten 10-90 CD study was a 3" p-type conductive substrate with 25nm SiO_2 grown via PECVD and 50nm ZnO grown via PLD as discussed in Section 3.3.1. The ZnO was post-deposition baked. TiW was sputtered as discussed in Section 3.3.2.4 at 1000Å thick. A layer of PMGI SF-11 PR was spun on the wafer at 4000 rpm for 30 seconds at a ramp of 200 rpm and baked for 10 minutes at 250°C. A second PR layer of 1805 was spun on the wafer at 4000 rpm for 30 seconds at a ramp of 200 rpm and baked for 75 seconds at 110°C. Using the Ohmic mask from the QuickLot process, the PR was exposed for 1.9 seconds on the MA6 mask aligner ($10mW/cm^2$, λ = 365-405 nm), developed with 1:5 ratio of 351:DI at 500 rpm for 30 seconds, rinsed with DI at 500 rpm for 30 seconds, and dried with N_2. The SF-11 was then exposed to DUV for 200 seconds

with the 1805 acting as the mask, developed with 101 developer for 120 seconds, rinsed in DI, and dried with N_2. The sample was scored into several pieces for multiple SiO_2 RIE chemistry tests observing the features listed above in the introduction of Section 3.5. The samples were submitted to SEM imaging for FIB cross-sectioning for structural layer observation.

3.5.5 Tungsten

The wafers used for the tungsten CD study were 3" p-type conductive substrate with 25nm SiO_2 grown via PECVD and either 50nm or 75nm ZnO grown via PLD as discussed in Section 3.3.1. The 50nm ZnO wafer was post-deposition baked. The 75nm ZnO wafer was not post-deposition baked. Tungsten was sputtered as discussed in Section 3.3.2.1 at 1000Å thick. A layer of PMGI SF-11 PR was spun on the wafer at 4000 rpm for 30 seconds at a ramp of 200 rpm and baked for 10 minutes at 250°C. A second PR layer of 1805 was spun on the wafer at 4000 rpm for 30 seconds at a ramp of 200 rpm and baked for 75 seconds at 110°C. Using the Ohmic mask from the QuickLot process, the PR was exposed for 1.9 seconds on the MA6 mask aligner (10mW/cm^2, λ = 365-405 nm), developed with 1:5 ratio of 351:DI at 500 rpm for 30 seconds, rinsed with DI at 500 rpm for 30 seconds, and dried with N_2. The SF-11 was then exposed to DUV for 200 seconds with the 1805 acting as the mask, developed with 101 developer for 120 seconds, rinsed in DI, and dried with N_2. The sample was scored into several pieces for multiple SiO_2 RIE chemistry tests observing the features listed above in the introduction of Section 3.5. The samples were submitted to SEM imaging for FIB cross-sectioning for structural layer observation.

3.6 Device Fabrication and Direct Current Testing

Two types of devices were fabricated in this section: Those with channels defined using optical lithography, and those with channels defined using e-beam lithography. Both channel types were subtractively etched using their respective masks and patterns under the SiO_2 RIE chemistry. Within the types, the fabrication process remained the same for each type of contact material. Furthermore, the results of the etch and CD studies in Sections 3.4 and 3.5, respectively, were applied to eliminate contact materials which did not have ideal etch rates and/or RIE profiles. The optical and e-beam defined devices were tested for their DC capabilities using similar parameters as outlined in Section 3.6.3. The results from each channel type were compared to the AFRL standard lift-off procedure, whose channels are also optically-defined, the results of which were previously collected through the works of AFRL engineers. The devices fabricated in this section follow a similar, two-finger design shown in Figure 3.3. The sources (S), drain (D), and a non-functional gate (G) probe pad are labeled. The L_c and W_c, also labeled, are the same for each finger.

3.6.1 Optically-Defined Subtractive Etch Devices

Utilizing the results from the CD study in Section 3.5, optically-defined devices were fabricated and tested. By fabricating optically-defined devices and using RIE for subtractive channel opening, device testing can be conducted and their operation verified before attempting to fabricate costlier and more time-consuming e-beam devices. For sample preparation, 75nm ZnO was deposited via PLD and annealed as discussed in

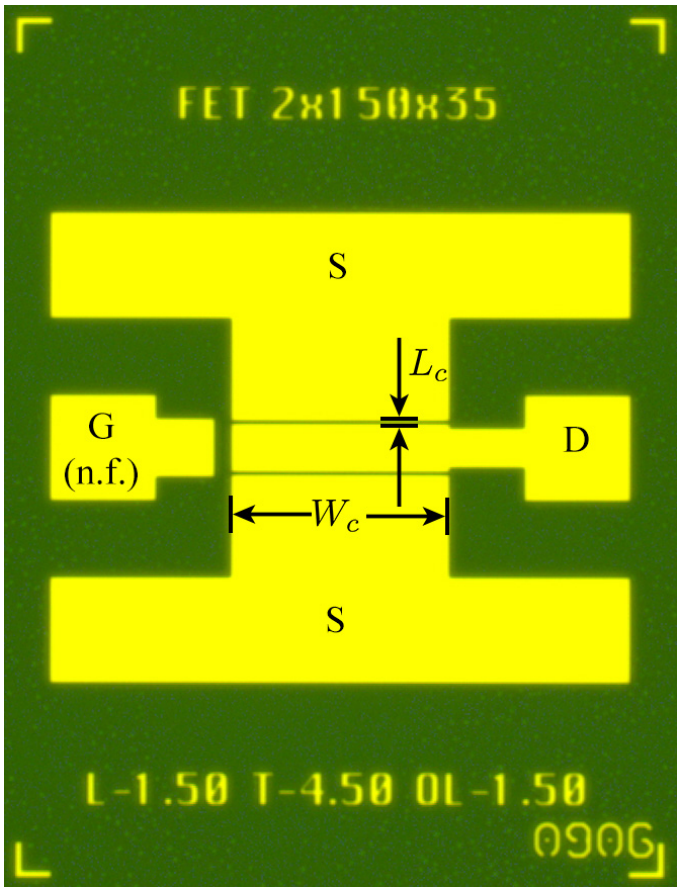

Figure 3.3: The two-finger thin-film transistor layout utilized in the thesis research

Section 3.3.1 on 25nm SiO_2 and 3" silicon wafer (Figure 3.4a). Lastly, the contact material was deposited as discussed in Section 3.3.2 (Figure 3.4b).

For device fabrication, mesas from the QuickLot process were defined using 1813 PR, spun on at 4000 rpm for 30 seconds at a ramp of 4000 rpm, and baked for 75 seconds at 110°C. After developing and ashing, the field device access material was etched away using the SiO_2 etch chemistry in the RIE 790 tool. The field ZnO was then etched away using a 1:1000 ratio of DI:HCl for 25 seconds for device isolation and the remaining 1813 PR (Figure 3.4c). A Ti/Pt/Au/Ni (200/300/2500/200Å) metal liftoff was then evaporated

with patterned SF-11 and 1805 PR, lifted off with the tape liftoff method, the remainder PR stripped, and the sample and ashed for cleaning (Figure 3.4d). The device channels were opened using the metal pattern as a mask in the SiO_2 etch chemistry. The Ni top does not etch in the SiO_2 etch chemistry (Figure 3.4e). The resulting devices were then tested as outlined in Section 3.6.3.

3.6.2 Electron Beam Lithographically-Defined Subtractive Etch Devices

After optically-defined devices were fabricated, tested, and verified as functional devices, e-beam-defined devices were fabricated and tested using a similar process. The e-beam devices in the QuickLot process do not have mesa-isolated active regions, and the processing steps result in all optical devices within the reticule sacrificed. For sample preparation, 75nm ZnO was deposited via PLD and annealed as discussed in Section 3.3.1 on 25nm SiO_2 and 3" p-type silicon wafer (Figure 3.4a). Lastly, the contact material was deposited as discussed in Section 3.3.2 (Figure 3.4b).

For device fabrication, the e-beam devices were initially defined with a negative Ohmic PR pattern from the QuickLot process composed of SF-11 and 1805. The SF-11 was selected for its robustness under the SiO_2 etch chemistry. With the negative Ohmic mask, the e-beam devices within the reticule do not have channels defined. The field device access material was etched away with the SiO_2 etch chemistry and the field ZnO was etched away using a 1:1000 ratio of DI:HCl for 25 seconds for device isolation (Figure 3.4c). A Ti/Pt/Au (200/300/3500Å) metal liftoff was prepared using SF-11 and 1805 PR and patterned with the positive Ohmic mask from the QuickLot process. The e-beam devices in the positive mask have a 3μm channel opening, allowing for e-beam

writing between the metal stack (Figure 3.4d). The metal was lifted off with the tape liftoff method, the remainder PR stripped, and the sample ashed for cleaning. The device channels were opened using ZEP-520A PR written with e-beam lithography under the SiO_2 RIE chemistry (Figure 3.4e). The resulting devices were then tested as outlined in Section 3.6.3.

3.6.3 Testing

The devices detailed above were tested for their DC capabilities and compared to the standard lift-off process employed by AFRL. The standard lift-off process involves adhering a Ti/Pt/Au (200/300/3500Å) stack directly to the ZnO active layer and using the standard tape lift-off method for channel definition. An issue that arises with this process is the ZnO channel top surface is damaged when the metal stack combined with the PR used for pattern definition is pulled away.

The DC characterization was performed using a fully-automated Cascade probe system. An HP4142 parameter analyzer gathered DC measurement data. The DC I-V family of curves was captured by sweeping V_{ds} from 0 to 10V in 0.2V increments for $0\text{V} < V_{gs} < 10\text{V}$, $\Delta V_{gs} = 1\text{V}$ and measuring the resultant drain current I_{ds}. The current density J_{ds} and transconductance g_m were captured by sweeping the gate voltage V_{gs} from 0 to 10 to 0V in 0.05V increments while maintaining the drain-source voltage V_{ds} constant at 10V.

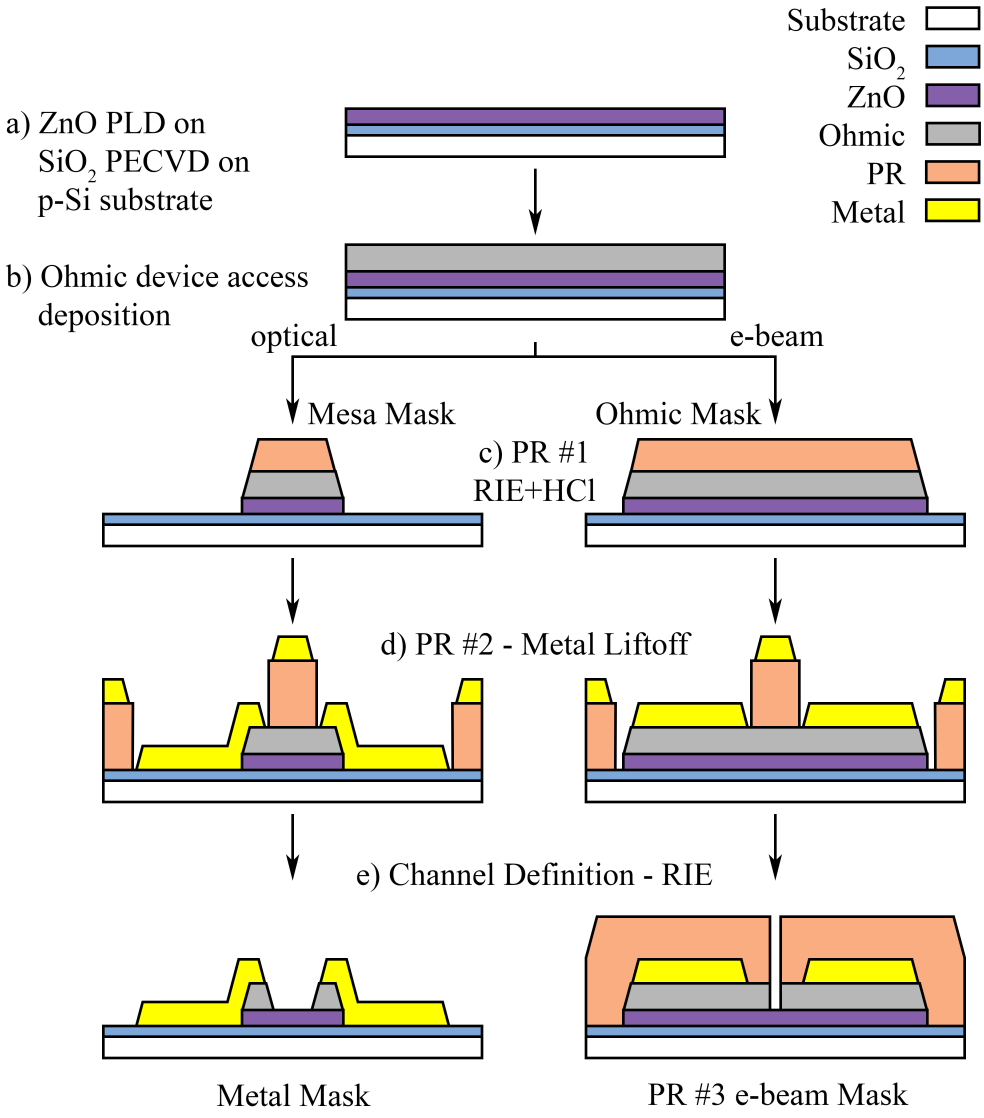

Figure 3.4: Process Flow Diagram for Optical and e-Beam Devices

3.7 Summary

This chapter outlined the steps executed in data gathering for the thesis research. In the next chapter, the results of these steps are presented.

IV. Results and Analysis

4.1 Introduction

THE Results and Analysis chapter presents the data captured through executing the methodology steps presented in Chapter 3. To present the results in an orderly and logical way, this chapter is divided into section correlating to their respective Chapter 3 sections. These sections include the results of the etch study, followed by the critical dimension study, and finally device fabrication and testing.

4.2 Etch Study

The results of the etch selectivity study are presented in this section. To establish an effective etch selectivity, an etch study on ZnO was conducted first to obtain an etch rate (ER) under the SiO_2 etch chemistry. Independent etch studies of the target contact materials were conducted next. Lastly, to ensure mask integrity throughout a subtractive etch process for accurate channel dimension definition, etch studoes on polydimethylglutarimide (PMGI) SF-11, a deep ultra-violet (DUV)-reactive photoresist (PR), and ZEP-520A, an electron beam (e-beam) PR, were also conducted.

4.2.1 Zinc Oxide

ZnO was known to be difficult to etch under the SiO_2 etch chemistry. A thicker film of ZnO was deposited via pulsed-laser deposition (PLD) at 209 nm to generate larger step height measurements, thus reducing the inherent profilometer noise (see Section 3.4.2 and Figure 3.1). However, larger step heights demand longer etch times provided all other

reactive-ion etching (RIE) variables remain constant. An n-type silicon mask 76.2 nm thick was used to define the etch boundary. Due to the n-Si mask etching in the SiO_2 chemistry, severe undercutting was observed in the 50W ZnO etch which complicated determining the etch boundary. Another ZnO sample was prepared for the 50W data point measurement using evaporated Ni dots 1 mm in diameter and 1000Å thick. Ni is known to be resistant to etching under the SiO_2 etch chemistry. The 50W data point in Table 4.1 was etched for 3 hours and resulted in an etch depth of ~25Å. The etch depth was determined from averaging several Ni mask step heights before and after etching using the profilometer. The results of the ZnO RIE study are listed in Table 4.1. A graphical representation of these data is presented in Figure 4.1.

Table 4.1: Zinc Oxide SiO_2 RIE Chemistry Etch Rate

Power (W)	Bias (V)	ZnO ER (Å/min)
200	461	23.8
150	388	12.6
100	297	5.02
50	175	0.138

4.2.2 Contact Materials

This section discusses the etch study results of all contact materials discussed in Chapter 3. A summary of all contact material etch rates and selectivities to ZnO

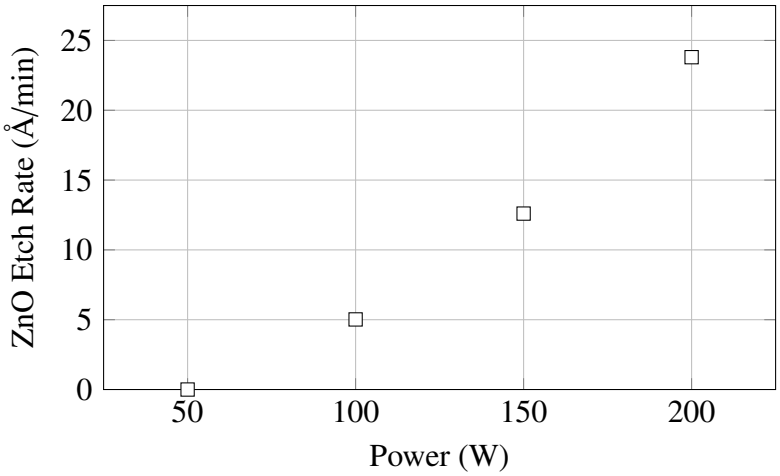

Figure 4.1: Zinc Oxide Etch Rate vs. Power

discovered in this section are presented in Figures 4.2 and 4.3, respectively, while individual tables and graphs of each contact material are presented in Appendix B and Appendix C, respectively, for further clarity. As shown in Figure 4.2, the materials with the highest etch rates across all SiO_2 RIE chemistry powers included nanocrystalline silicon (nc-Si), TiW, and W. This resulted in higher estimated selectivity to ZnO compared against other contact materials studied, as confirmed in Figure 4.3.

4.2.2.1 Silicon

The SiO_2 etch used at Air Force Research Laboratory (AFRL) has a known etch rate for SiO_2. To establish an effective ER for nc-Si, the first material in the etch study was n-type silicon (n-Si). Establishing an n-Si etch rate allowed for estimating the time needed to etch partially through the nc-Si, ensuring accurate step height and etch rate calculations. This step is necessary as only 1160Å nc-Si thin-film material was available to etch, and a

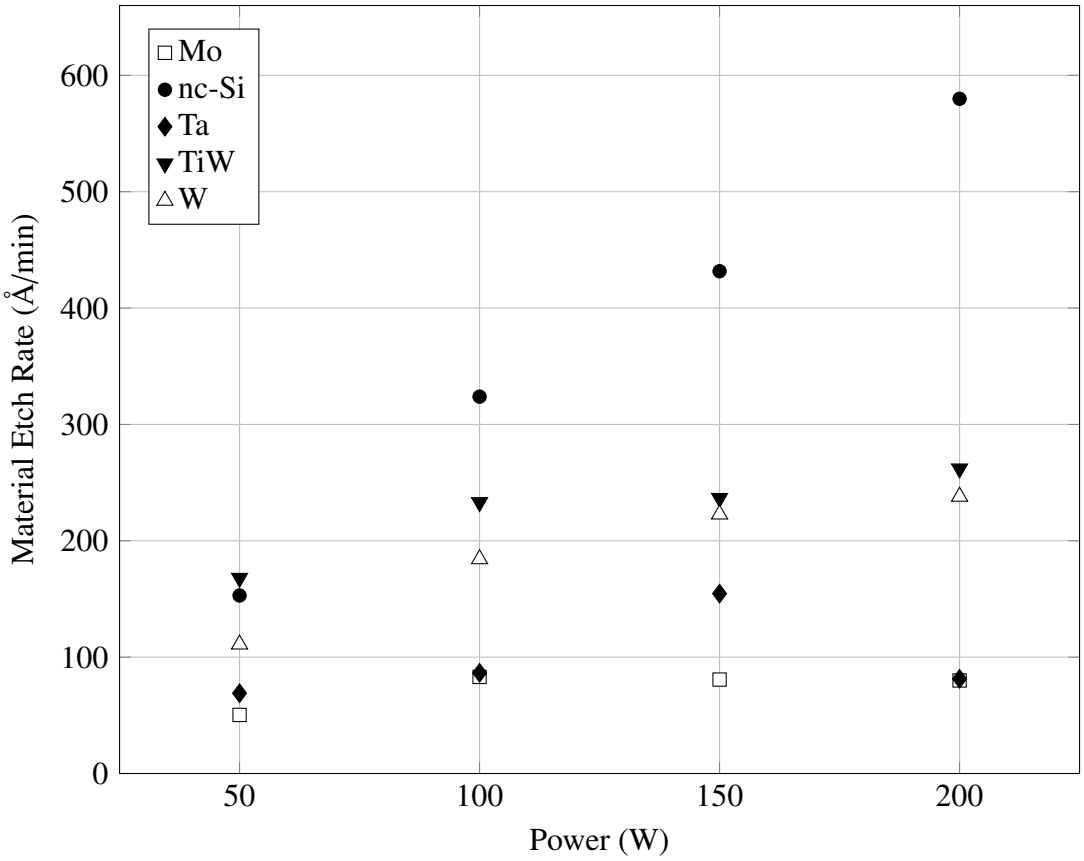

Figure 4.2: Material Etch Rate vs. SiO_2 RIE Chemistry Power

limited number of samples of nc-Si were provided. Etching through the film would result in inaccurate etch rate measurements, and etching too little through the film would introduce inaccuracies in the step-height measurements on the profilometer due to its resolution and inherent noise. An example of profilometer noise can be seen in Figure 3.1.

The results of the silicon RIE study are listed in Table B.1. Each etch was conducted at four minutes independently at 200, 150, 100, and 50W RIE powers. The DC bias is dependent on the radio frequency (RF) power. Due to the direct current (DC) bias

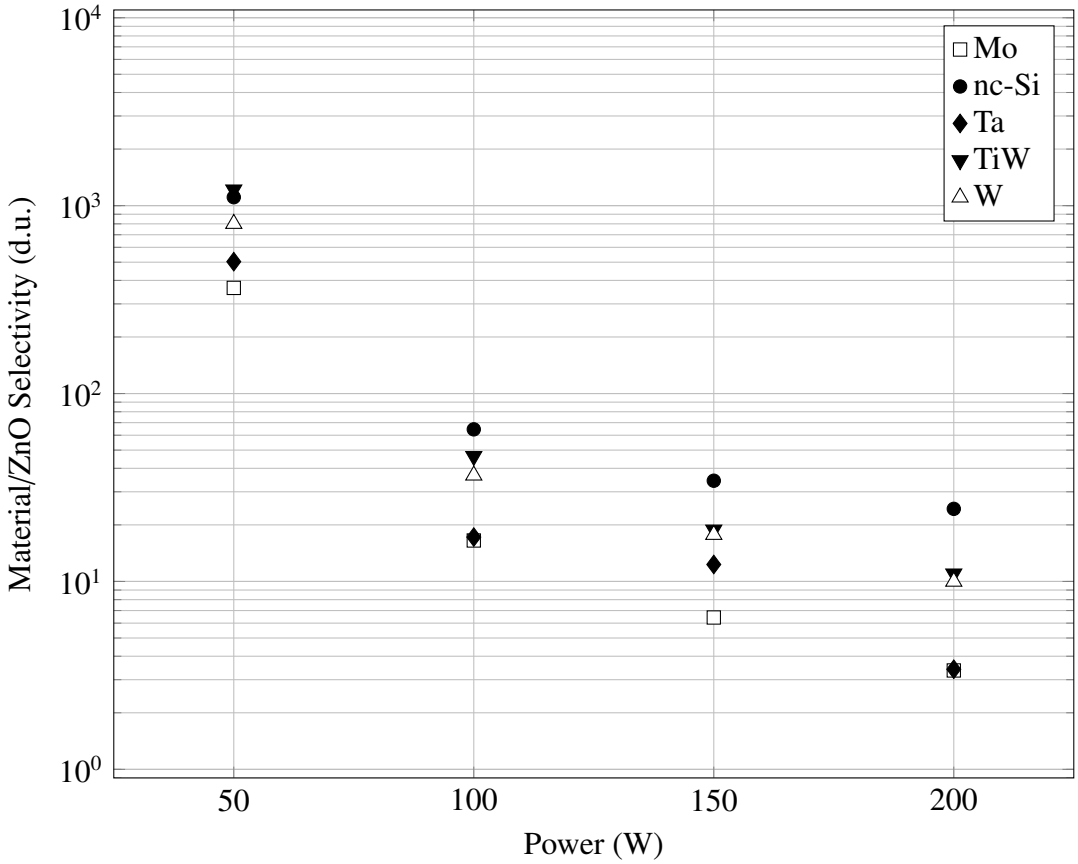

Figure 4.3: Estimated Material Selectivity to ZnO vs. SiO_2 RIE Chemistry Power

dropping significantly at 50W, the overall etch rate for this sample was significantly lowered and reduced by over half from 100W.

4.2.2.2 Molybdenum

The results of the molybdenum RIE study are listed in Table B.2. A graphical representation of these data is presented in Figures C.1 and C.2. It can be observed the molybdenum etch rate is strongly dependent on etch time. While the etch time slope was linear with respect to RIE power, the resultant etch rates were not. In an independent trial at 150W RIE power for 2:45, the etch rate was faster than at 200W — 97Å/min against

81Å/min, respectively. Repeating this trial resulted in a different etch rate as reported in Table B.2. Additionally, the etch rates for molybdenum were amongst the slowest recorded during this phase of the research and thus the worst estimated selectivity to ZnO can be predicted as confirmed in Figures 4.2 and 4.3. The molybdenum etch study results suggest unpredictability in etch rates and thus complications can arise during subtractive etch processes. The unpredictable etch rates will cause repeatability issues in future device fabrication.

4.2.2.3 Nanocrystalline Silicon

The results of the nc-Si RIE study are listed in Table B.3. A graphical representation of these data is presented in Figures C.3 and C.4. The silicon etch study results from Section 4.2.2.1 were applied to predict similar results for nc-Si and allowed for efficiently using the limited nc-Si samples provided. The nc-Si contact material displays good correlation to RIE power, with a negative, near-linear trend as RIE power decreases. These results suggest etch times for various material thicknesses can be accurately predicted and repeatably executed.

4.2.2.4 Tantalum

The results of the Ta RIE study are listed in Table B.4. A graphical representation of these data is presented in Figures C.5 and C.6. A logical correlation between Ta etch rate and RIE power is not observed in Figure C.5. Multiple trials at each etch power were conducted, with the resultant etch rate varying greatly with strong dependence on etch time. The results presented in Table B.4 are the deepest recorded step heights from the profilometer for each power to ensure accurate etch rates are reported. The Ta etch study

suggests a highly non-linear etch rate relationship with RIE power for the material. Etch times for various Ta thicknesses will be difficult to predict accurately. Furthermore, undesirable effects from inaccurately calculating etch times can appear, such as undercutting, not clearing the channel of all Ta, and/or consuming mask material.

4.2.2.5 Titanium Tungsten

The results of the TiW RIE study are listed in Table B.5. A graphical representation of these data is presented in Figures C.7 and C.8. The TiW contact material displays good etch rate correlation to RIE power in that etch rate decreases with power, with similar etch rates observed at 150 and 100W. These results suggest etch times for various material thicknesses can be accurately predicted and repeatably executed. TiW also has higher estimated selectivity than Ta and Mo due to its higher etch rates across the four RIE powers observed. Therefore, TiW is a good candidate for subtractive etch channel definition against ZnO due to its high predicted selectivity across the four RIE powers.

4.2.2.6 Tungsten

The results of the W RIE study are listed in Table B.6. A graphical representation of these data is presented in Figures C.9 and C.10. Tungsten displays excellent etch rate correlation to RIE power, with decreasing etch rate with RIE power. These results suggest etch times for various material thicknesses can be accurately predicted and repeatably executed. Tungsten also has higher estimated selectivity than Ta and Mo due to its higher etch rates across the four RIE powers observed. Therefore, W is a good candidate for subtractive etch channel definition against ZnO.

4.2.3 Photoresist

The results of the SF-11 RIE study are listed in Table B.7. A graphical representation of these data is presented in Figure C.11. The etch rate of SF-11 was calculated using Equation (3.1) with TiW and W as the etched material. The samples prepared contained ZnO underneath the etch material, which was assumed to perform an etch-stop. The sample size remained similar to others within the etch study. Each RIE power was executed once per etch material, and multiple data points for each RIE power were collected via profilometer within their respective samples and averaged. Finally, the SF-11 etch rates for TiW and W etch materials were averaged within their corresponding RIE power categories. These averages were then extrapolated across all target materials to estimate their selectivity to SF-11. The estimated material selectivity to SF-11 is shown in Figure 4.4. The graph suggests the SiO_2 RIE chemistry transitions from physical to chemical etch properties at 150W where the selectivity is lowest. Actual material etch rates for a full wafer will vary from observed etch rates of the smaller samples. These actual etch rates may be slower or faster depending on the size of the wafer, the surface area of exposed target material, and the material itself.

The results of the ZEP-520A RIE study are listed in Table B.8. A graphical representation of these data is presented in Figure C.12. The etch rate of each contact material was divided by the etch rate of ZEP-520A for each RIE power to estimate the etch selectivity. The estimated etch selectivities of all target contact materials to ZEP-520A are presented in Figure 4.5. As previously noted, actual material etch rates for a full wafer will vary from observed etch rates of the smaller samples. These actual etch

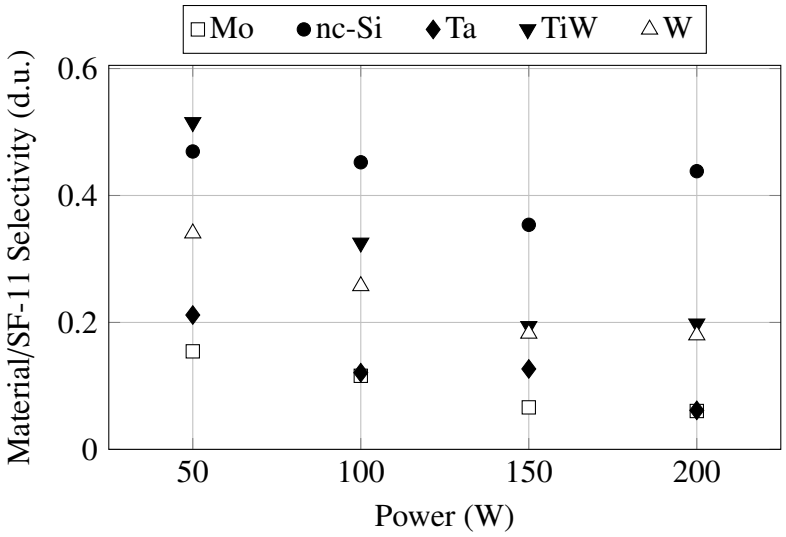

Figure 4.4: Estimated Material Selectivity to SF-11 vs. SiO_2 RIE Chemistry Power

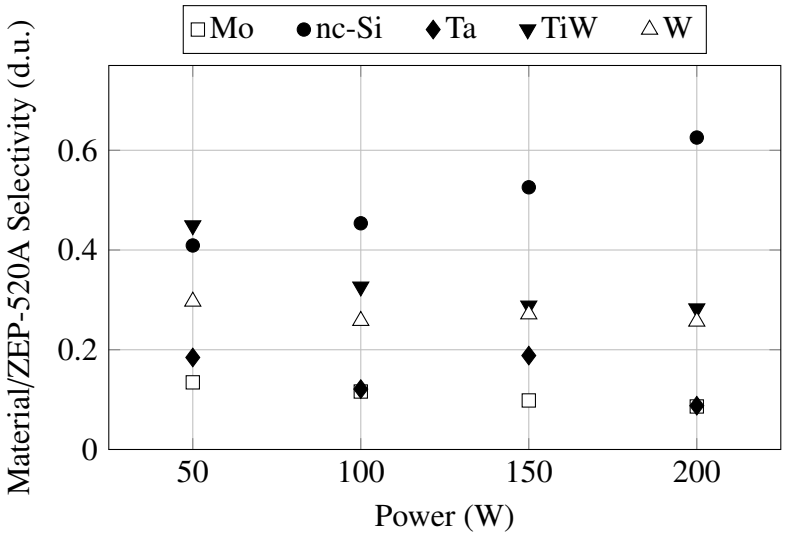

Figure 4.5: Estimated Material Selectivity to ZEP-520A vs. SiO_2 RIE Chemistry Power

rates may be slower or faster depending on the size of the wafer, the surface area of exposed target material, and the material itself.

4.3 Critical Dimension Study

The results of the critical dimension (CD) study are discussed in this section. Each contact material was observed under optical microscopy and scanning electron microscope (SEM) for mask integrity, etch profile, and edge acuity. The SEM has a focused ion beam (FIB) function, which was used for cross-sectioning of patterned devices. Of the four available powers used in the RIE, the 200 and 50W-etched devices were observed under SEM for cross-sectioning unless otherwise noted. This reduced the number of samples observed to the extreme powers, allowing for reducing time-consuming FIB processing. Additionally, this allowed for eliminating materials not displaying ideal results at these extreme powers from further investigation.

4.3.1 Molybdenum

As shown in Figure 4.6a, the SF-11 PR was consumed during the dry-etch procedure due to slow etch rates of Mo under 200W RIE power. A similar outcome was observed when the RIE power was altered to 50W, as shown in Figure 4.6b. Under optical microscope observation, the 150 and 100W samples displayed resist cracking and dull edge definition, suggesting a similar compromised mask outcome as the 200W sample. Therefore, time-consuming FIB cross-sectioning SEM images of the 150 and 100W RIE powers were not conducted. An independent etch study for Mo may be necessary to identify ideal RIE parameters for controllable and repeatable device fabrication. However, due to its extremely slow etch rate at all powers observed, there may not exist a PR that will maintain its integrity during the dry etch while offering similar device scaling capabilities. Other parameters of the Mo film may need to be adjusted, such as film

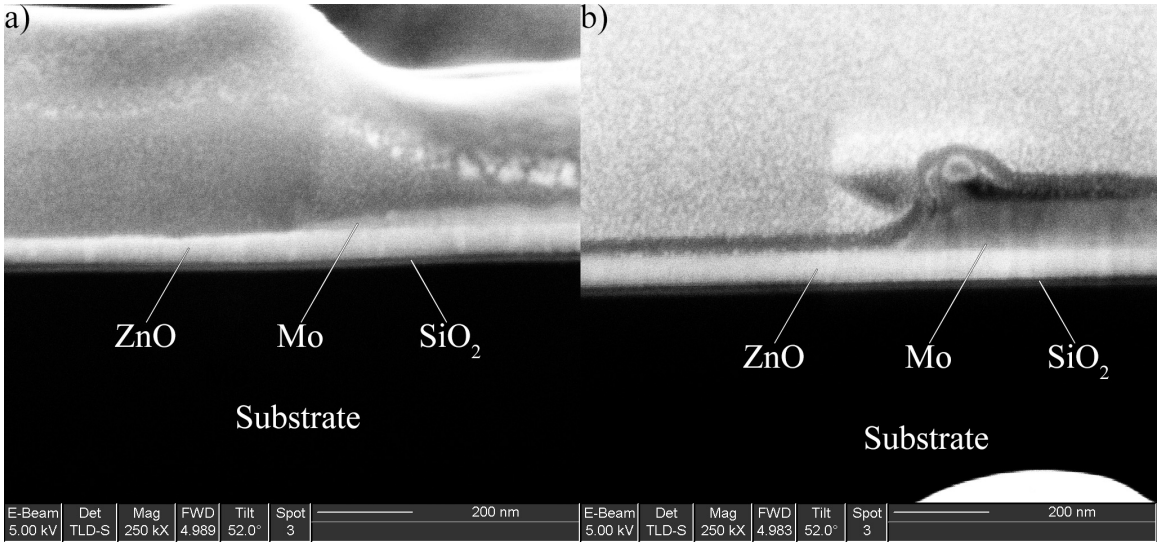

Figure 4.6: Mo Cross-Section at RIE Power a) 200W and b) 50W

thickness (thinning) at the expense of ρ_s, alloying, or other deposition and sputtering modifications. As these parameters are outside the thesis scope, Mo was henceforth eliminated as a viable candidate for subtractive channel definition in this thesis.

4.3.2 Nanocrystalline Silicon

The initial nc-Si samples provided by the University of Toledo were deposited at 1160Å film thickness with a 1000Å SiO_2 dielectric layer between it and the p-type 6" Si substrate. The etch chemistry utilized is specifically for anisotropically etching SiO_2. Therefore, an etch-stop layer did not exist beneath the nc-Si. 1813 PR was selected for masking for the CD study due to its predicted ability to maintain structural integrity throughout the calculated etch times for all RIE powers while etching nc-Si.

Figure 4.7 demonstrates a good example of how, as RIE power decreases, the plasma etch becomes less physical and more chemical due to higher free-flowing gases within the

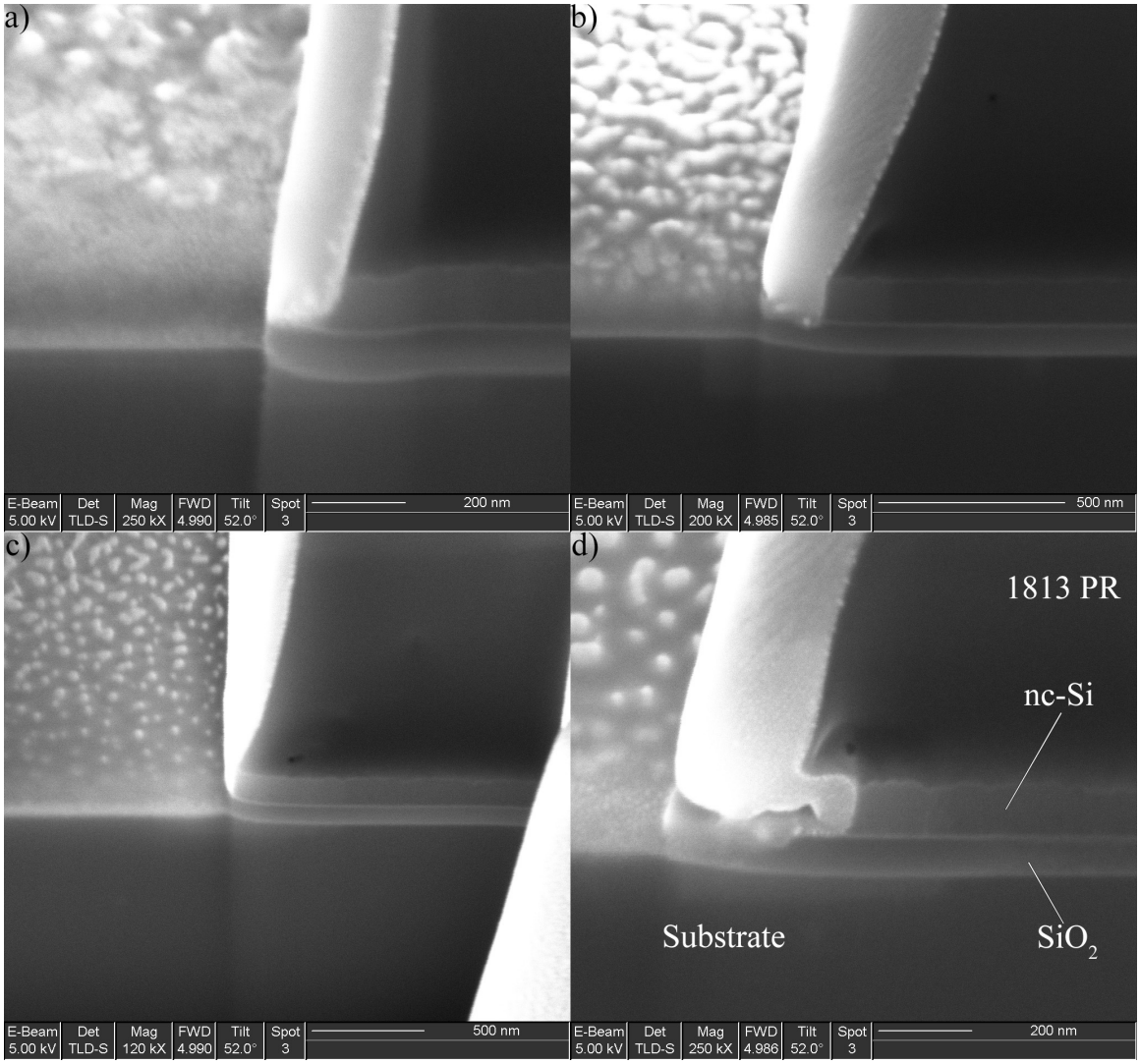

Figure 4.7: nc-Si Cross-Section at RIE Power a) 200W, b) 150W, c) 100W, and d) 50W

chamber and lower plasma interaction at the surface. A “foot” was observed at RIE power of 200W, as shown in Figure 4.7a. A foot would have an adverse effect on completely etching the channel open for sub-micron device dimensions. Severe mask undercutting at RIE power of 50W was observed for the nc-Si sample, as shown in Figure 4.7d. While undercutting can be useful in certain applications, repeatable CDs will be difficult to

obtain for channels defined with e-beam lithography. Furthermore, material structures defined with e-beam lithography which undercut the PR mask when dry-etched will have inaccurate device dimensions and, due to the possibility of material redeposition, result in devices which exhibit leakage and/or fringe current through the conduction channel. Therefore, the 200 and 50W RIE powers should be carefully considered with nc-Si if selected for future device fabrication. The nc-Si 150 and 100W RIE powers yielded more interesting and useful results for the thesis research because their corresponding nc-Si etch profiles maintain good edge acuity. These RIE powers were therefore considered for subtractive channel definition in Section 4.4.

4.3.3 Tantalum

Due to its similar etch rate to Mo in Section 4.3.1 at 200W RIE power, the SF-11 PR mask for Ta was consumed during the dry etch, shown in Figure 4.8a. The Ta-ZnO interface etch profile displays mask undercutting at 50W as shown in Figure 4.8b. While undercutting can be useful in certain applications, repeatable CDs will be difficult to obtain for channels defined with e-beam lithography. Furthermore, material structures defined with e-beam lithography which undercut the PR mask when dry-etched will have inaccurate device dimensions and, due to the possibility of material redeposition, result in devices which exhibit leakage and/or fringe current through the conduction channel. All four RIE power samples were observed under optical microscope, and residual Ta remained upon the field ZnO for each. Residual Ta will propagate into further processing complications, such as micro-masking of ZnO during device isolation or device performance issues, such as channel shorting or fringe current. These results suggest that

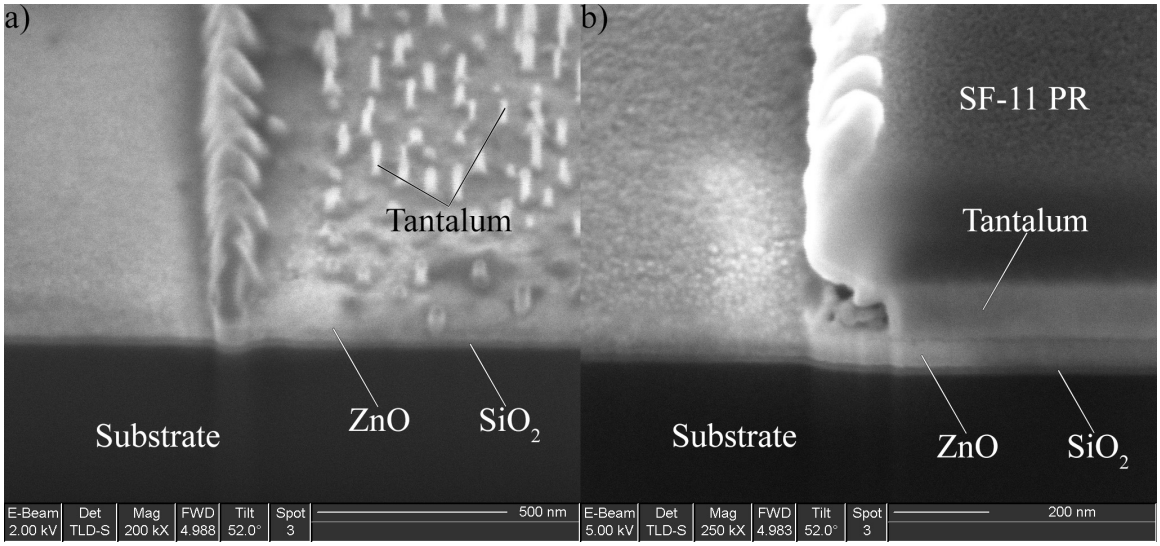

Figure 4.8: Ta Cross-Section at RIE Power a) 200W and b) 50W

ideal etch results do not exist for the SiO_2 etch chemistry in its present configuration across the four target RIE powers observed in this thesis. An independent etch study for Ta may be necessary to identify ideal RIE parameters for controllable and repeatable device fabrication. However, due to time constraints and thesis scope, non-linear etch rates observed in Section 4.2.2.4, and residual metal remaining after RIE, Ta was eliminated as a viable candidate for subtractive channel definition in this thesis.

4.3.4 Titanium Tungsten

As TiW was amongst the materials with the highest predicted etch selectivity to ZnO in the research, FIB cross-section etch profiles were captured for all four RIE powers. The SF-11 mask for the 100W was compromised as shown in Figure 4.9c. This result is an anomaly that requires further investigation. In all four RIE powers, either the PR may have delaminated from the TiW or an unknown PR-TiW surface interaction under RIE is

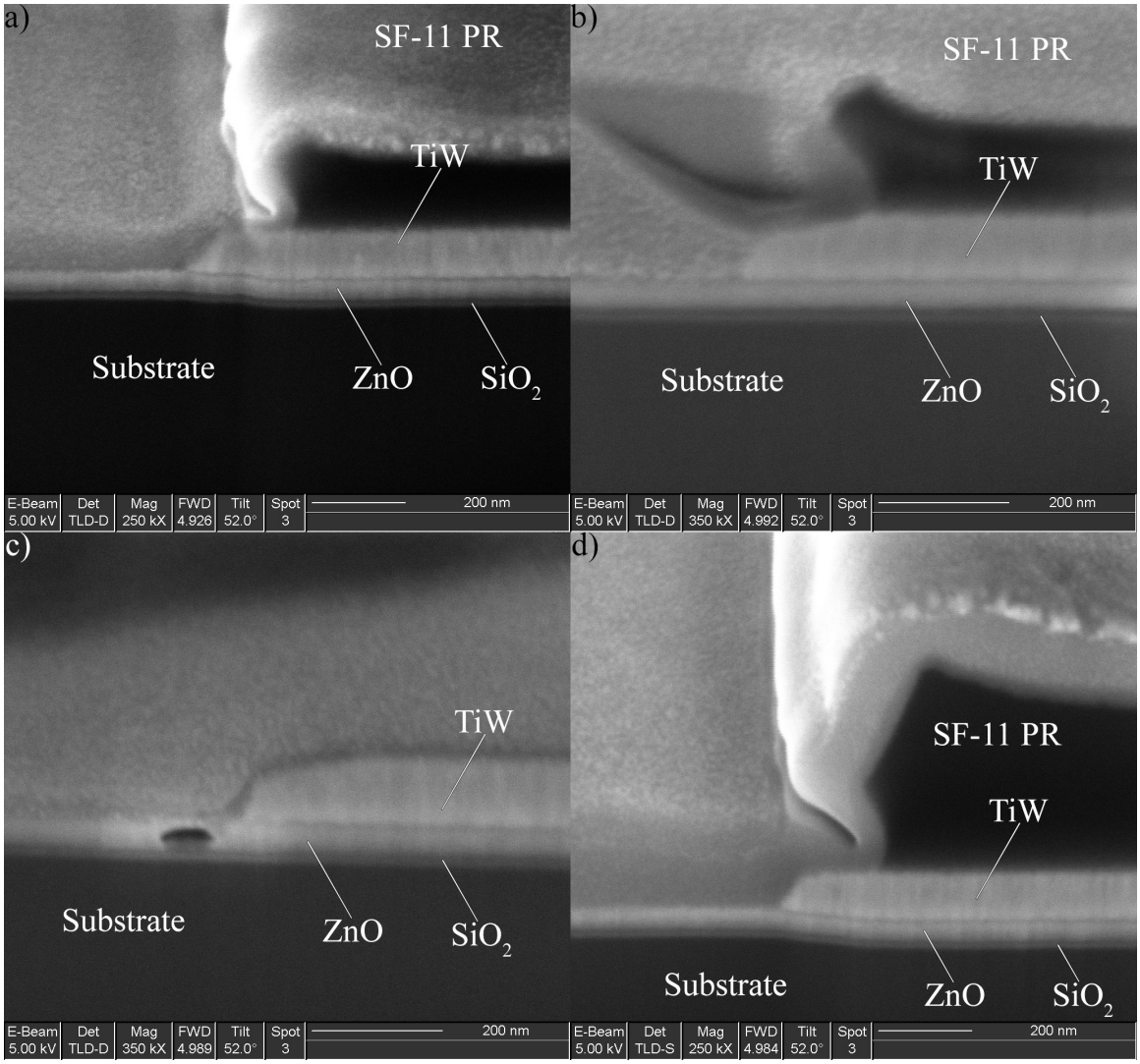

Figure 4.9: TiW Cross-Section at RIE Power a) 200W, b) 150W, c) 100W, and d) 50W

occurring at the boundary. Contact thinning near the channel edge begins to occur. This thinning may or may not have a direct impact on device performance due to increased resistance. Regardless, this PR issue can cause undesirable results in repeatably defining gate channel CDs and further investigation outside of the thesis scope is required to determine the cause.

Furthermore, all RIE power samples were observed under optical microscope, and the 50W sample displayed residual TiW remaining upon the field ZnO. A TiW sample wafer was prepared for fabrication and testing in Section 4.4 at 100W RIE power, but complications arose during device isolation due to unanticipated TiW micro-masking of ZnO. The residual TiW on this wafer could compromise device performance via channel shorting. The 200 and 150W RIE powers may reduce the residual TiW remaining upon the ZnO, but the expected etch selectivities to ZnO are significantly lower and a direct device performance comparison cannot be made to other materials at their ideal RIE power of 100W in Section 4.4. TiW requires further investigation and an optimized process for subtractively etching device channels.

4.3.5 Tungsten

As tungsten was amongst the materials with the highest predicted etch selectivity to ZnO in the research, FIB cross-section etch profiles were captured for all four RIE powers. The FIB cross-section images are displayed in Figure 4.10. The 200, 150, and 100W RIE powers display excellent edge acuity in maintaining the etch boundary as defined by the SF-11 PR. The 50W sample also displays excellent edge acuity, however tungsten was either redeposited or not completely etched within the channel area as shown in Figure 4.11. This can cause inaccurate channel dimensions or the inability to completely subtractively etch the channel open.

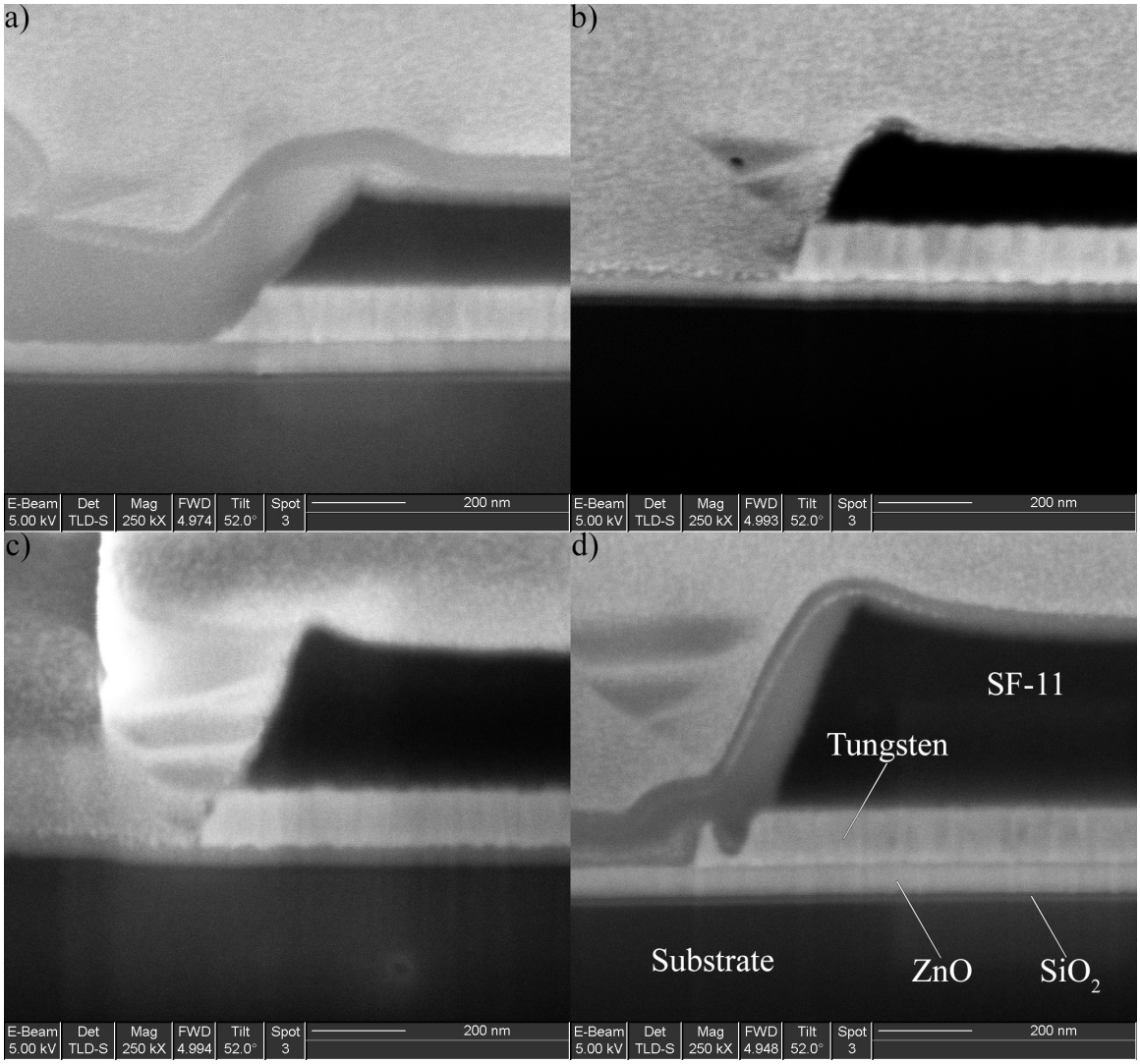

Figure 4.10: W Cross-Section at RIE Power a) 200W, b) 150W, c) 100W, and d) 50W

4.4 Device Fabrication and Direct Current Testing

4.4.1 Optically-Defined Subtractive Etch Devices

It was discovered upon channel definition through RIE the devices exhibited high leakage current and that a 250°C hot plate bake for 10 minutes reduced the leakage current to undetectable levels. This suggested the SiO_2 RIE chemistry is damaging the surface or

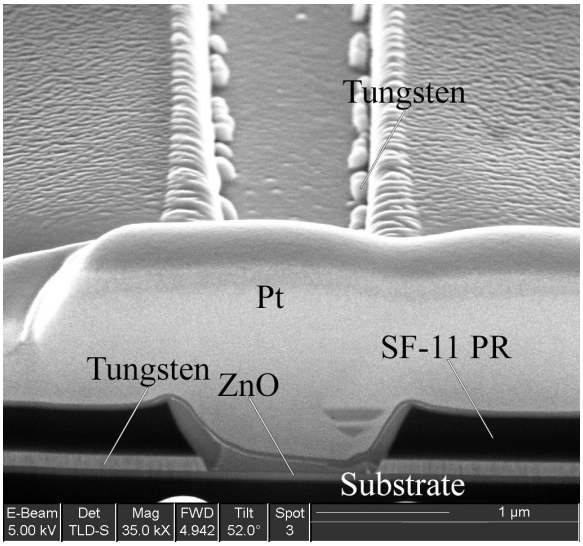

Figure 4.11: Tungsten Cross-Section at RIE Power 50W. Note tungsten remaining in channel.

other phenomenon are happening during the reaction. The SiO_2 RIE chemistry could be affecting the ZnO top surface in a similar manner used for plasma surface treatment before contact deposition in other research groups [32, 47]. Further experiments are required to determine which chemical reactions or surface interactions are causing the device leakage current. These experiments are outside the thesis scope. The best RIE power resulting in good edge acuity and etch selectivity amongst the remaining materials of interest, nc-Si and W, was at 100W and thus selected for use throughout this section.

4.4.1.1 Nanocrystalline Silicon

The results reported in this section are captured after the 250°C bake. The devices are W_c = 300µm across two finger gates. The subtractively etched devices with nc-Si device access material demonstrated a higher r_{on} average (~2×) across the sample wafer when compared to the standard lift-off process (377Ω vs. 213Ω, respectively). The i_{max} current

was also lower — 50 mA for the subtractively etched nc-Si devices against 87 mA for the lift-off process. The I_{on}/I_{off} ratio was lower — 4.1×10^4 against 1.2×10^6. The knee voltage V_{knee} was calculated 4.8V against 4.2V for the lift-off devices. These results could be due to the surface damage resulting from the SiO_2 RIE chemistry, which has not yet been characterized. However, the nc-Si material has higher resistivity to the Ti/Pt/Au metal contact scheme utilized in the lift-off process, and this higher resistivity could also be a contributing factor.

A Sony Tekronix 370A programmable curve tracer was used to manually test the devices. Using the nominal gate lengths and measuring the current of one gate at V_{ds} = 10V and V_{gs} = 10V, these subtractively etched devices show current scaling similar to lift-off devices reported elsewhere [3]. Using the best fit equation calculated through these few data points and assuming the current in both fingers are equivalent under similar biasing conditions, a L_c = 100nm device would scale to J_{ds} = 938mA/mm for a two-finger device. Lift-off devices have been biased with V_{ds} as much as 14V and V_{gs} as high as 16V, and therefore higher current density can be extrapolated from these devices under those conditions. The results of CD scaling are presented in Figure 4.14.

4.4.1.2 Tungsten

The optically-defined, subtractive etch devices with tungsten-ZnO contacts were fabricated in the same manner as their nc-Si counterparts. 500Å of W was deposited for these devices. The results of DC testing were inconclusive. The ZnO channel exhibited high leakage current and the devices did not pinch off following the 250°C hot plate bake.

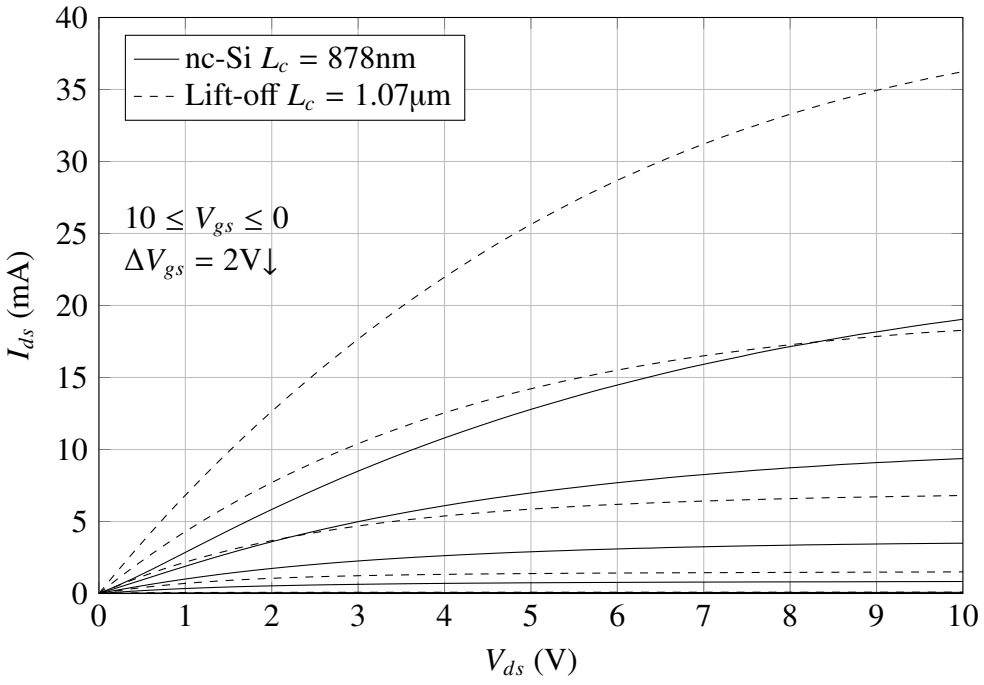

Figure 4.12: Representative DC I-V Curves nc-Si Subtractive Etch vs. AFRL Lift-off

This result could be due to a fabrication error. Further investigation into these results is necessary.

4.4.2 Electron Beam Lithographically-Defined Subtractive Etch Devices

4.4.2.1 Nanocrystalline Silicon

Due to the poor etch profile results presented in Section 4.3.2, the 200 and 50W RIE powers were eliminated from further investigation. While both 150 and 100W displayed desirable etch profiles, the 100W RIE power has the advantage of higher selectivity to ZnO and was therefore selected for subtractively etching channels defined with e-beam lithography. Due to the limited availability of nc-Si samples, an e-beam trial was conducted on the initial samples provided by the University of Toledo, with nc-Si

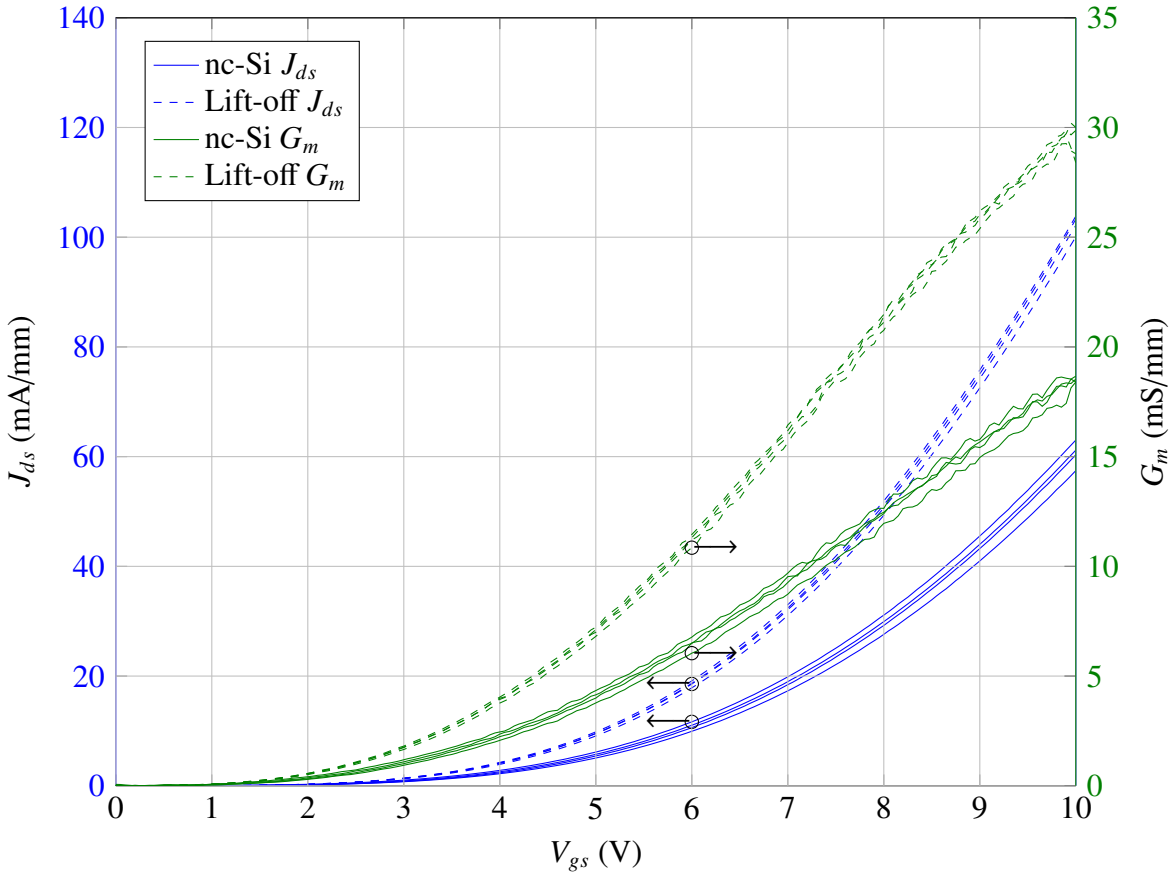

Figure 4.13: Current Density and Transconductance nc-Si Subtractive Etch vs. Lift-off

thin-film 1160Å thick with a 1000Å SiO_2 dielectric layer between it and the p-type Si substrate. The etch chemistry utilized is specifically for anisotropically etching SiO_2. Therefore, an etch-stop layer did not exist beneath the nc-Si.

A single dosage and dosage bias spread was conducted using a JEOL JBX-6300FS e-beam lithography tool for SEM analysis on viable e-beam parameters. The column bias was 100 keV. The e-beam trial was also conducted using a double-thickness layer of ZEP-520A PR, calculated from the etch study (Section 4.2.3) as necessary for mask integrity for 1160Å nc-Si, and analyzed for integrity. The smallest L_c achieved was 157nm

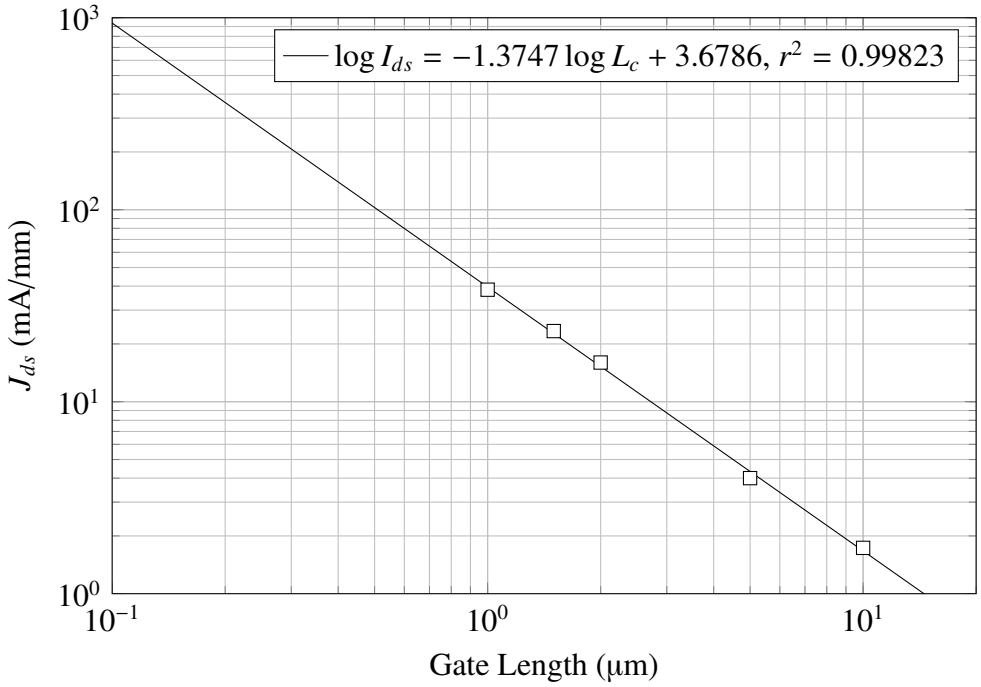

Figure 4.14: Current Density Scaling of nc-Si Subtractive Etch Devices

as shown in Figures 4.15 and 4.16. The nc-Si at the top of the film measured 172nm. The ZEP-520A PR measured 493nm at the top. Using the etch rate of nc-Si at 100W RIE power from Section 4.2.2.3, the calculated etch time with a 30% over-etch (OE) was 4:40. During this etch time, the ZEP-520A was calculated to etch to 3670Å from 7000Å for double-thickness ZEP-520A PR. However, the ZEP-520A PR etched faster than anticipated to 2390Å, and therefore a triple-thick PR stack would be necessary for completely opening the device channel on a functional device sample deposited with a thicker, 2100Å film of nc-Si.

Based upon this data, the smallest gate length extrapolates J_{ds} collected in Section 4.4.1.1 to 505mA/mm. By observing the etch profile in Figure 4.16, it is not

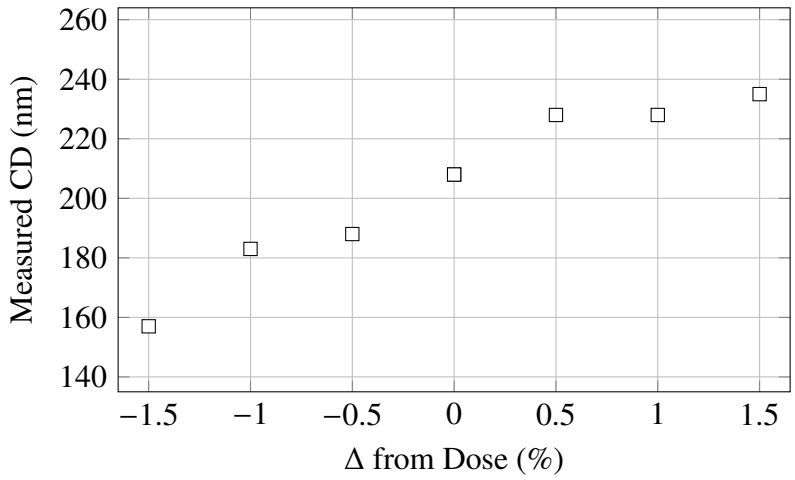

Figure 4.15: Nanocrystalline Silicon e-Beam Measured CD vs. %Δ from Dose = 350μC/cm^2

unreasonable to predict smaller gate lengths, such as 100nm, can be achieved. Therefore, the J_{ds} = 938mA/mm for a two-finger, W_c = 150μm, and L_c = 100nm device as calculated previously would be possible.

4.4.2.2 Tungsten

A triple-thick stack of ZEP-520A PR was anticipated to etch the nc-Si device access material sample. For experimental continuity and results comparison, the tungsten sample was prepared with a triple-thick stack of ZEP-520A PR. However, the resist cracked due to stress from the device features underneath. The cracks appeared above non-critical device areas, and, after being examined under SEM, it was determined the written e-beam channel features had not lost integrity post-development. The devices were etched under a timed SiO_2 etch chemistry at 100W for 7:03, for a 30% OE. The DC I-V family of curves data was captured both pre- and post-250°C 10 minute bake, shown in Figure 4.17.

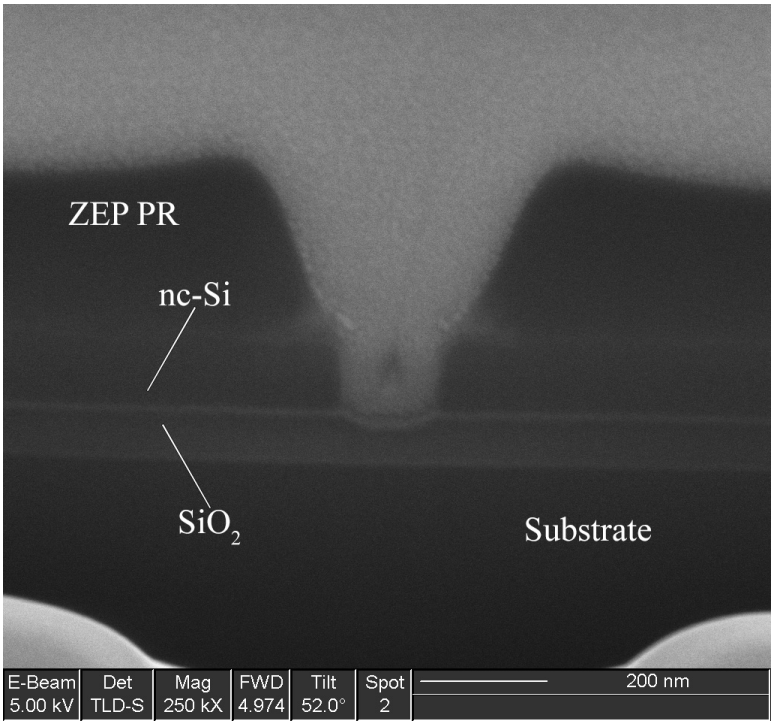

Figure 4.16: Nanocrystalline Silicon e-Beam Lithography Trial Results. L_c = 157nm

The J_{ds}(max) was 28mA/mm and G_m(max) was 12 mS/mm on a typical device across the wafer. The current density displayed a hysteresis effect, indicative of internal capacitance storing during forward V_{ds} sweep and discharging during negative sweep. Figure 4.17 provides a good example of device leakage current before a 10 minute, 250°C hot-plate bake and how the effects are minimized after the bake. Upon SEM observation and FIB cross-sectioning, it was observed the ZnO active channel layer had etched during the final processing steps. In most areas of the channel, the remaining ZnO had been removed completely as shown in Figure 4.18a. The SiO_2 underneath the ZnO in this area was not etched, suggesting the SiO_2 RIE chemistry was not responsible for ZnO thinning. In some areas of the channel, the ZnO was continuous between the source and drain but

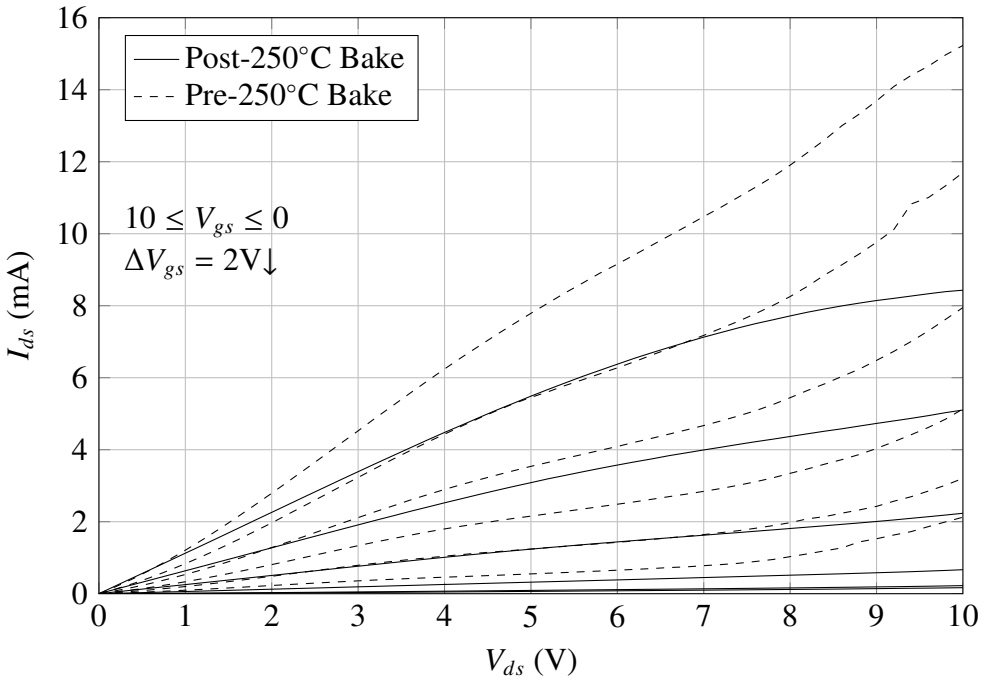

Figure 4.17: Best e-Beam Tungsten Device DC I-V Curves, Pre- and Post-250°C Bake

had beem thinned as shown in Figure 4.18b, justifying the switching capability of the device yet very low I_{ds} results, as shown in Figure 4.17 when compared to Figure 4.12 previously. Investigating further into the reasoning behind the ZnO etching during the final processing steps is required. One hypothesis is as follows: The 1165 PR stripper used to remove the ZEP-520A PR combined form a mild acid which would etch the ZnO. This hypothesis is justified because the ZEP-520A PR is the only chemical difference between the subtractive optical and e-beam processes within Section 4.4. Furthermore, the ZnO etched isotropically and undercut the tungsten, indicative of a wet-etch on small grain-size structures rather than highly-directional plasma etching. Lastly, the channel

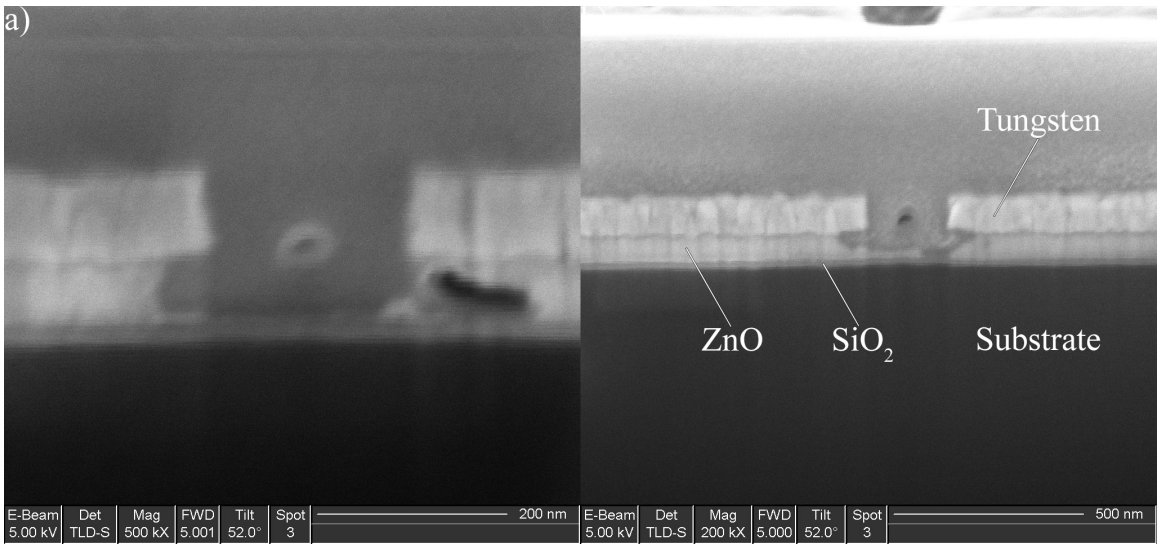

Figure 4.18: Cross-Section of E-Beam-Defined, Tungsten-Access Channel, a) ZnO completely removed b) ZnO thinned

area was protected until RIE followed by PR removal, indicating the PR removal process itself compromised the active channel layer instead of previous processing steps.

While the device performance was not ideal, the results are promising. The devices display I_{ds} steps with decreasing V_{gs} and trend toward a saturation region with higher V_{ds}. The devices also pinch-off, however with $I_{\text{on}}/I_{\text{off}}$ significantly lower than typically reported for the lift-off devices. The lower ratio is directly attributable to ZnO channel degradation and thinning; the channel layer then becomes a high-value resistor. Further process optimization and identifying fabrication steps which caused ZnO channel etching and rectifying those steps should result in excellent device performance in the future.

4.5 Summary

This chapter resulted in a complete etch study for several candidate device access materials under a SiO_2 RIE chemistry across four target RIE powers of 200, 150, 100, and 50W. The best estimated material selectivity to both ZnO and PR were determined to occur at the lower RIE powers of 100 and 50W. The materials with the highest estimated selectivity to ZnO, which included nc-Si, TiW, and W, displayed good edge acuity amongst the highest three RIE powers in the CD study, suggesting that 100W would be the ideal RIE power for device fabrication. Device channels with nc-Si and W access materials were subtractively etched and display promising results for achieving smaller CDs, higher I_{ds}, and higher J_{ds} compared to the standard AFRL lift-off devices.

V. Conclusions

5.1 Summary

The ultimate goal of this thesis, to identify a subtractive etch process with which to define the channel of ZnO thin-film transistors (TFTs), was met. A plasma-assisted etch (PAE) chemistry composed of a 40:3 ratio of CF_4:O_2 in a reactive-ion etching (RIE) tool was identified to have high selectivity to ZnO with certain contact materials and an etch study verified the results. The best selectivity results were estimated to occur with nanocrystalline silicon (nc-Si), titanium tungsten (10-90), and tungsten, with selectivities of 64, 46, and 37 dimensionless unit (d.u.), respectively, at 100W RIE power. An observation of the contact material/ZnO interface and etch profile showed good channel edge acuity for device scaling for each of these materials under the same RIE conditions. A subtractive etch process was executed with nc-Si and tungsten for device access with both optical and electron beam (e-beam) lithographically-defined channels and functional ZnO devices were obtained. The smallest critical dimension (CD) obtained was with nc-Si and measured 157nm, with good vertical sidewalls suggesting further device scaling with this contact material is obtainable. As a result, devices with nc-Si access material are predicted to achieve a current density J_{ds} of 938mA/mm at $V_{gs} = V_{ds} = 10$V, and additional biasing may result in further current density increases. Tungsten sidewalls were more perpendicular than nc-Si, but devices were non-functional due to unanticipated ZnO removal unrelated to the subtractive etch process. The tungsten channel observed measured ~200nm in length L_c.

5.2 Future Work

The ZnO contacts in this thesis are predicted to be Ohmic, but they have not been characterized for their barrier heights and specific contact resistance. Ohmic characterization should be accomplished to establish a baseline upon which further materials optimization can occur. These material optimizations include ZnO alloying such as IGZO, contact deposition parameter modification such as deposition rate, pre-deposition ZnO surface treatment using plasma, and post-deposition annealing conditions other than the standard process used at the Air Force Research Laboratory (AFRL). Furthermore, RIE parameters should also be considered, including gas flow rate, gas ratio, direct current (DC) bias, and chamber pressure. Continued research into new contact materials compatible with the SiO_2 RIE chemistry is also required. Different etch chemistries with the contact materials contained in this thesis also require investigation, provided they exhibit selectivity to ZnO. The chemical reaction equations for the contact materials in this thesis were not investigated.

In future experiments, a thinner layer of nc-Si should be deposited to reduce the RIE times required to subtractively etch for channel definition. The nc-Si was deposited at 2100Å for this thesis, which required a triple-stack of ZEP-520A photoresist (PR) limiting the smallest CD achievable with e-beam lithography. In reducing the nc-Si layer, single- or double-stack ZEP-520A PR can be utilized allowing for complete PR development at smaller CDs. Alternative PR materials to ZEP-520A could also be used, such as the thinner SF-5 PR for e-beam lithography writes. The most important next step is identifying the reason ZnO was removed when using e-beam lithography and ZEP-520A

PR. Solving this etching problem will allow for future e-beam defined, subtractively etched devices to be fully fabricated and tested, and possibly achieve X-band radio frequency (RF) performance from ZnO TFTs.

Appendix A: Elements and Element Compounds

Al	Aluminum
Ag	Silver
As	Arsenic
Au	Gold
CdSe	Cadmium selenide
CF_4	Carbon tetraflouride
Cu	Copper
KrF	Krypton flouride
H_2	Hydrogen
HCl	Hydrochloric acid
K	Potassium
Li	Lithium
Mo	Molybdenum
O and O_2	Oxygen
N and N_2	Nitrogen
Na	Sodium
Ni	Nickel
P	Phosphorus
PH_3	Phosphine
Pt	Platinum
Si	Silicon
SiH_4	Silane
SiO_2	Silicon dioxide
Ta	Tantalum
Ti	Titanium
TiW	Titanium tungsten alloy (10:90)
W	Tungsten
ZnO	Zinc oxide

Appendix B: Material Tables Expanded

B.1 Silicon

Table B.1: Silicon SiO_2 RIE Chemistry Etch Rate

Power (W)	DC Bias (V)	n-Si ER (Å/min)
200	460	500
150	391	425
100	304	309
50	185	133

B.2 Molybdenum

Table B.2: Molybdenum SiO_2 RIE Chemistry Etch Rate and Estimated ZnO Sel.

Power (W)	Bias (V)	Mo ER (Å/min)	Sel. (d.u.)
200	451	80	3
150	382	81	6
100	310	83	17
50	189	50	365

B.3 Nanocrystalline Silicon

Table B.3: Nanocrystalline Silicon SiO_2 RIE Chemistry Etch Rate and Estimated ZnO Sel.

Power (W)	Bias (V)	nc-Si ER (Å/min)	Sel. (d.u.)
200	460	580	24
150	391	432	34
100	310	324	64
50	187	153	1109

B.4 Tantalum

Table B.4: Tantalum SiO_2 RIE Chemistry Etch Rate and Estimated ZnO Sel.

Power (W)	Bias (V)	Ta ER (Å/min)	Sel. (d.u.)
200	452	81	3
150	382	155	12
100	310	86	17
50	192	69	503

B.5 Titanium Tungsten

Table B.5: Titanium Tungsten SiO_2 RIE Chemistry Etch Rate and Estimated ZnO Sel.

Power (W)	Bias (V)	TiW ER (Å/min)	Sel. (d.u.)
200	463	262	11
150	395	237	19
100	306	233	46
50	190	168	1216

B.6 Tungsten

Table B.6: Tungsten SiO_2 RIE Chemistry Etch Rate and Estimated ZnO Sel.

Power (W)	Bias (V)	W ER (Å/min)	Sel. (d.u.)
200	458	238	10
150	390	223	18
100	305	184	37
50	183	111	801

B.7 SF-11

Table B.7: SF-11 SiO_2 RIE Chemistry Etch Rate

Power (W)	Bias (V)	SF-11 ER (Å/min)
200	461	1323
150	395	1220
100	309	716
50	192	326

B.8 ZEP-520A

Table B.8: ZEP-520A SiO_2 RIE Chemistry Etch Rate

Power (W)	Bias (V)	ZEP-520A ER (Å/min)
200	463	927
150	397	821
100	313	714
50	207	374

Appendix C: Material Plots Expanded

C.1 Molybdenum

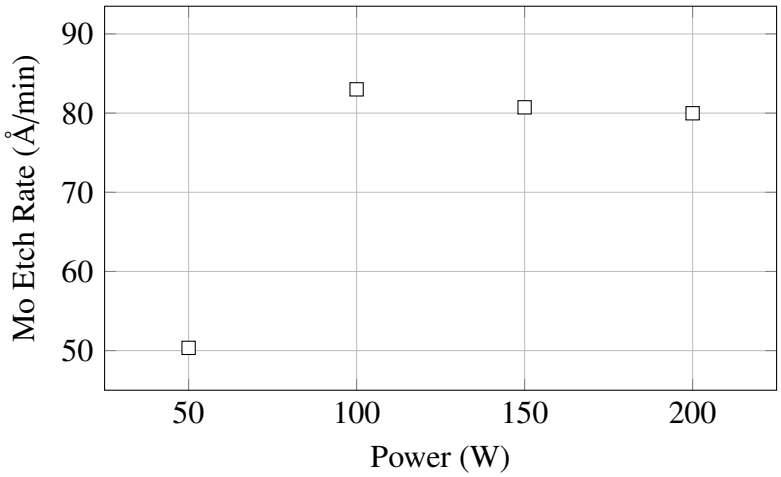

Figure C.1: Mo Etch Rate vs. SiO_2 RIE Chemistry Power

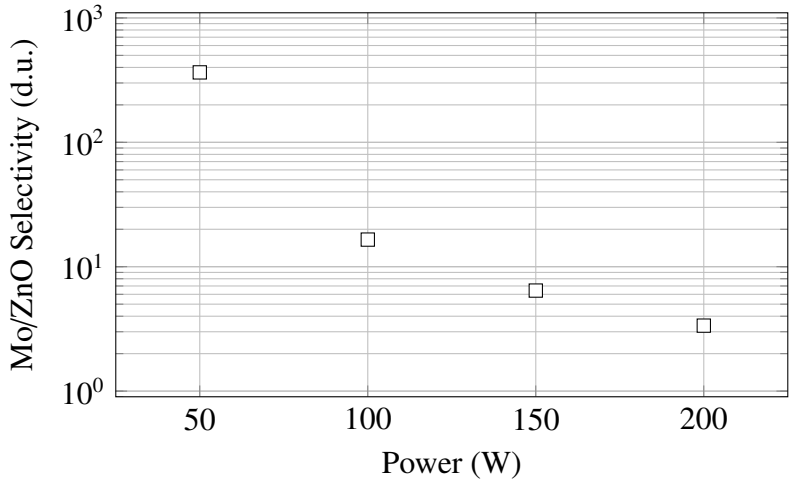

Figure C.2: Estimated Mo Selectivity to ZnO vs. SiO_2 RIE Chemistry Power

C.2 Nanocrystalline Silicon

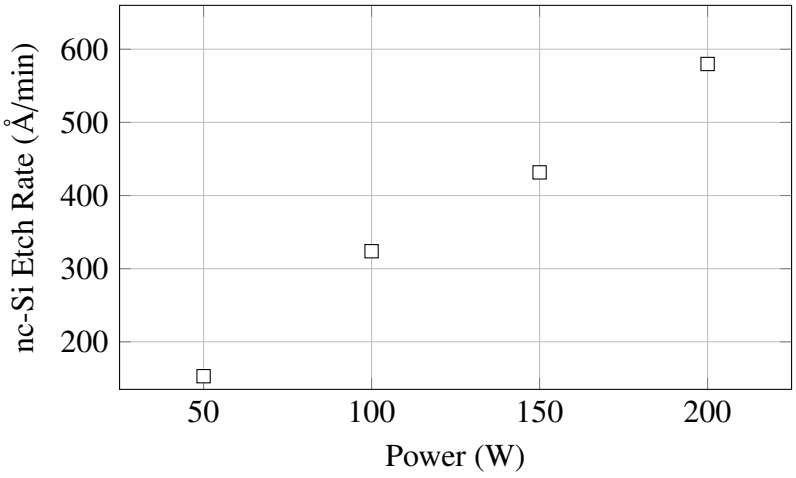

Figure C.3: nc-Si Etch Rate vs. SiO_2 RIE Chemistry Power

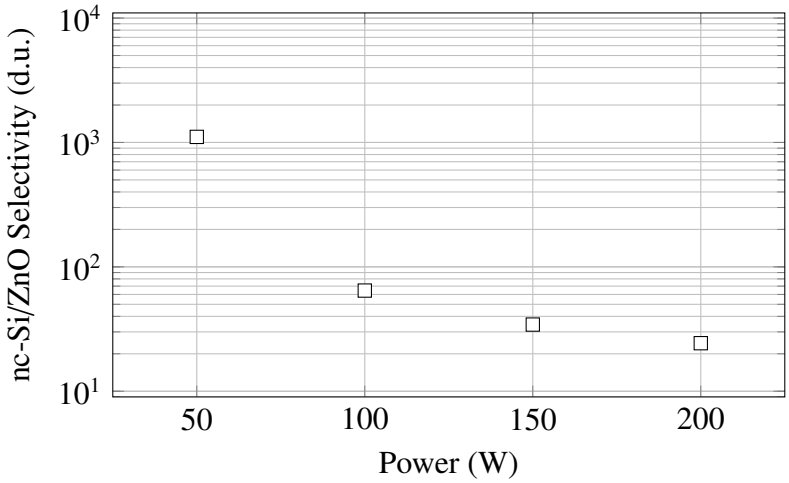

Figure C.4: Estimated nc-Si Selectivity to ZnO vs. SiO_2 RIE Chemistry Power

C.3 Tantalum

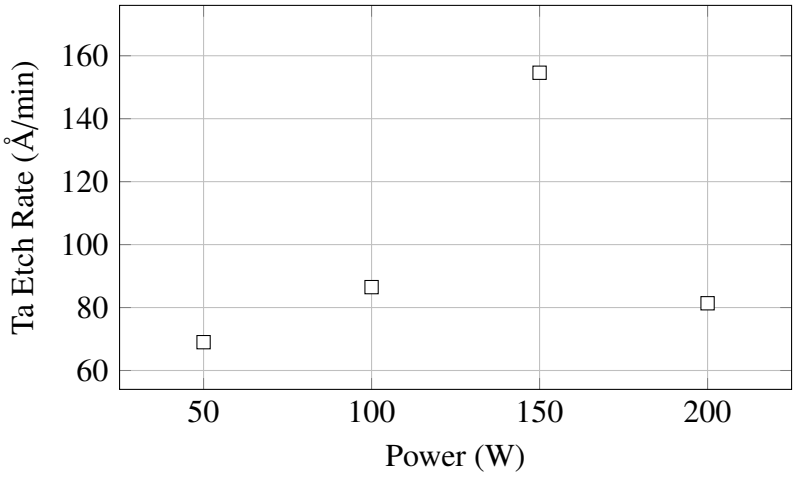

Figure C.5: Ta Etch Rate vs. SiO_2 RIE Chemistry Power

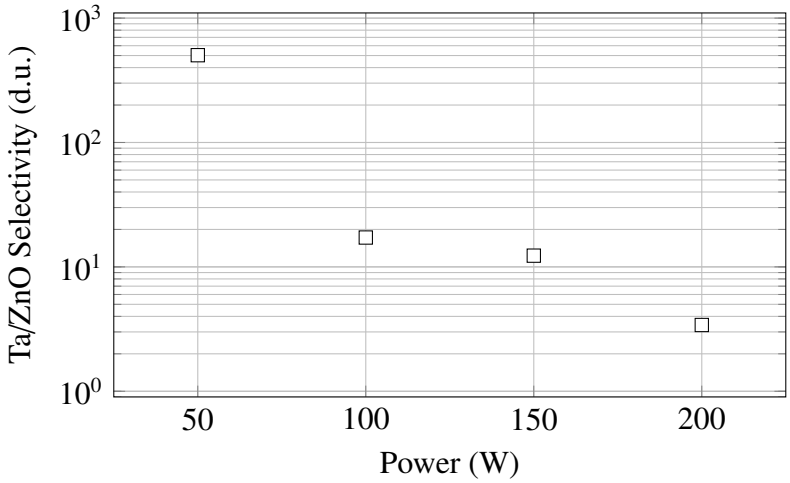

Figure C.6: Estimated Ta Selectivity to ZnO vs. SiO_2 RIE Chemistry Power

C.4 Titanium Tungsten

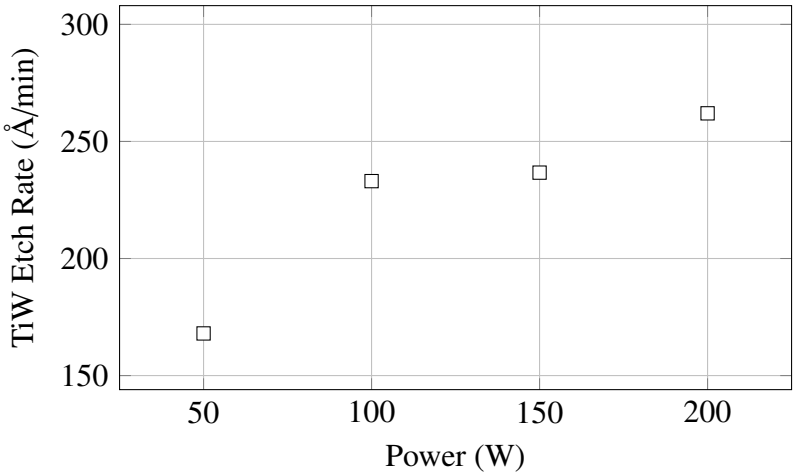

Figure C.7: TiW Etch Rate vs. SiO_2 RIE Chemistry Power

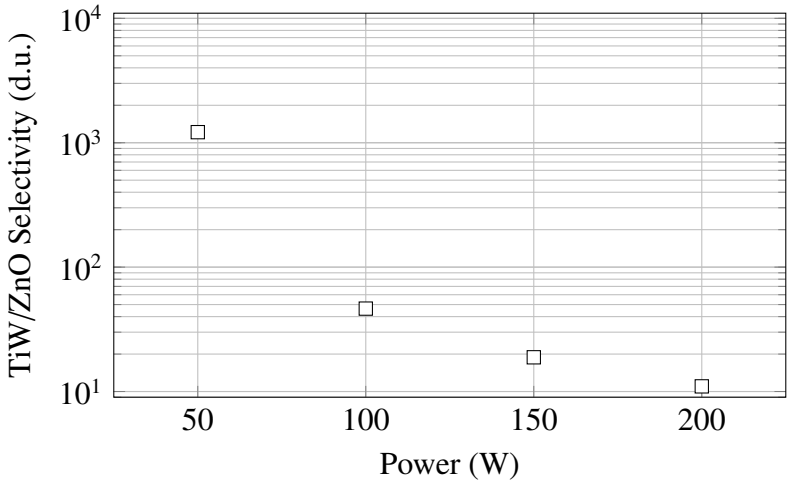

Figure C.8: Estimated TiW Selectivity to ZnO vs. SiO_2 RIE Chemistry Power

C.5 Tungsten

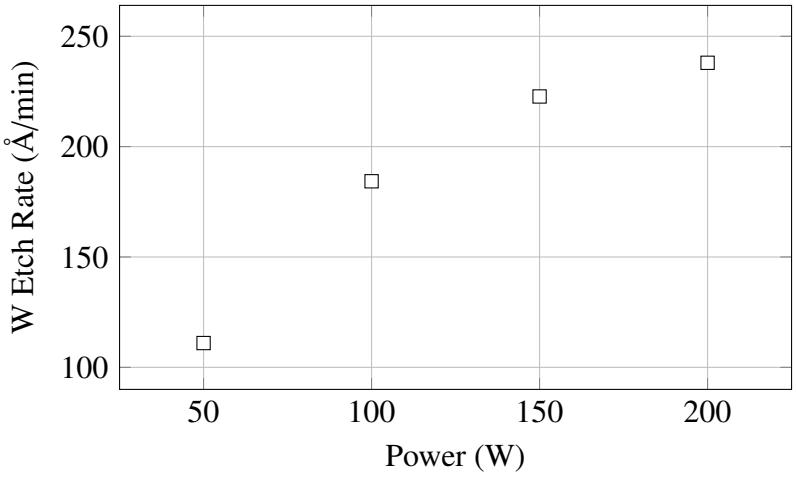

Figure C.9: W Etch Rate vs. SiO_2 RIE Chemistry Power

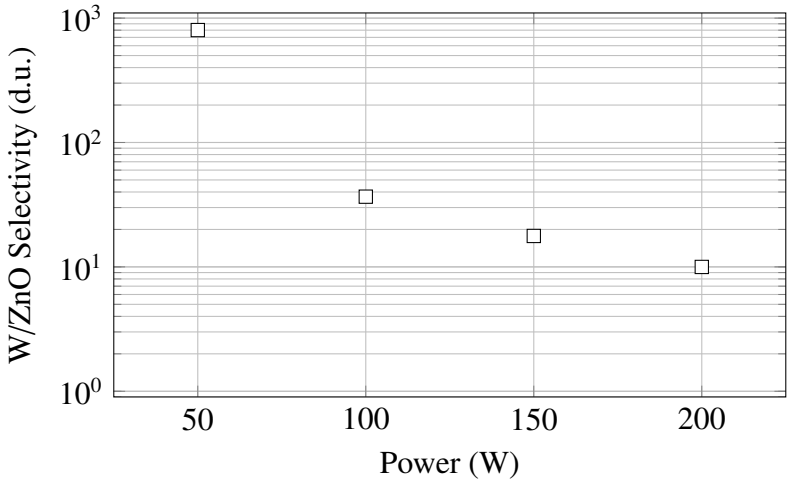

Figure C.10: Estimated W Selectivity to ZnO vs. SiO_2 RIE Chemistry Power

C.6 SF-11

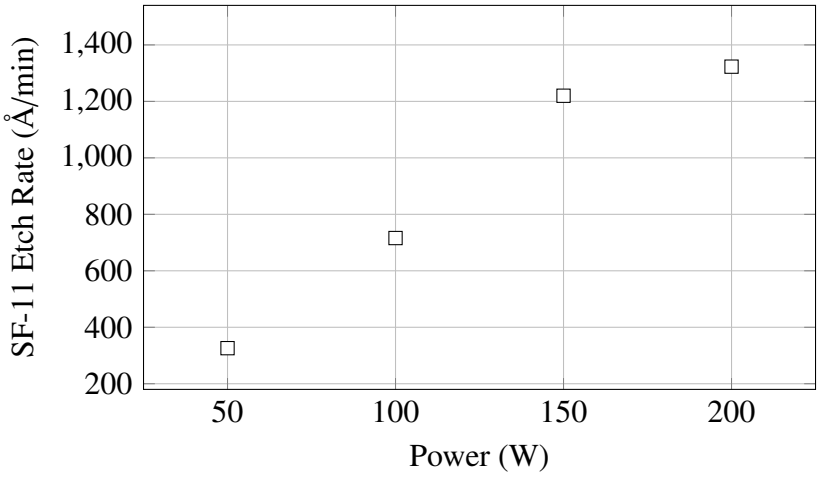

Figure C.11: SF-11 Etch Rate vs. SiO_2 RIE Chemistry Power

C.7 ZEP-520A

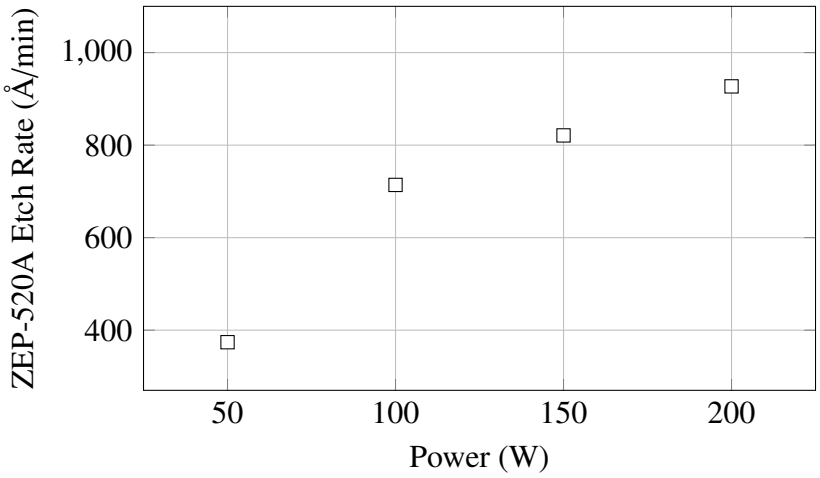

Figure C.12: ZEP-520A Etch Rate vs. SiO_2 RIE Chemistry Power

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Vita

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14. ABSTRACT

Recently, gigahertz RF performance has been demonstrated in zinc oxide (ZnO) TFT. However, the need arises for sub-micron channel length (Lc) dimensions to extend these results into X-band frequency range of operation. This thesis is a pioneering effort identifying device access materials to be selectively etched to ZnO via plasma-assisted etch (PAE) to avoid processing limitations from traditional optical lithography channel definition methods. A subtractive etch process using CF4/O2 gas mixture was completed with various Ohmic contact materials to ZnO providing foundational research upon which nano-scale, high-frequency ZnO thin-film transistors (TFTs) could be fabricated. Molybdenum, tantalum, titanium tungsten 10-90, and tungsten metallic contact schemes to ZnO are investigated for their etch selectivities to ZnO and etch profiles. Tungsten displayed promising device scalability results with excellent aspect ratio and 200nm Lc. A new semiconductor-semiconductor contact interface to ZnO using nc-Si is initially reported with 15mA/mm current density and 18mS/mm transconductance. Nc-Si also displays promising scaling results through the subtractive etch process defined with e-beam lithography. Results included 157nm channel length, high aspect

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ZnO, thin-films, device scaling, subtractive etch, plasma-assisted etch

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